Real-Time Extension to the RISC-V Advanced Interrupt Architecture

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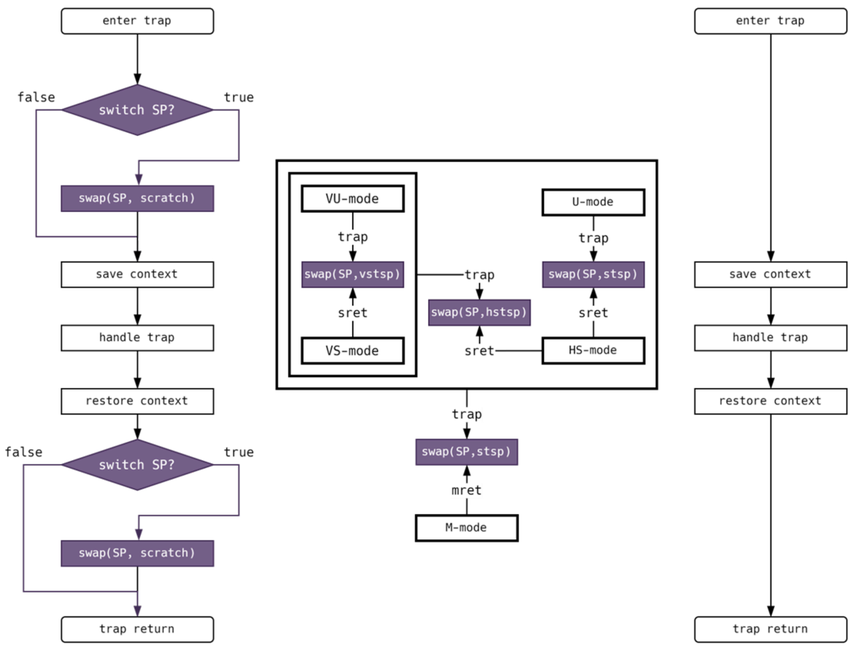
Motivation

Requirement	RISC-V AIA
Real-Time (deterministic low latency) interrupts	No
Multi-core configuration support	Yes
Virtualization support	Yes
Inter-processor interrupt	Yes
RISC-V ISA Compliance, incl. H-extension	Yes
Unified programming model	Yes
Flexible interrupt routing	Yes
Bus-less single core configuration support	No

Proposed Extensions:

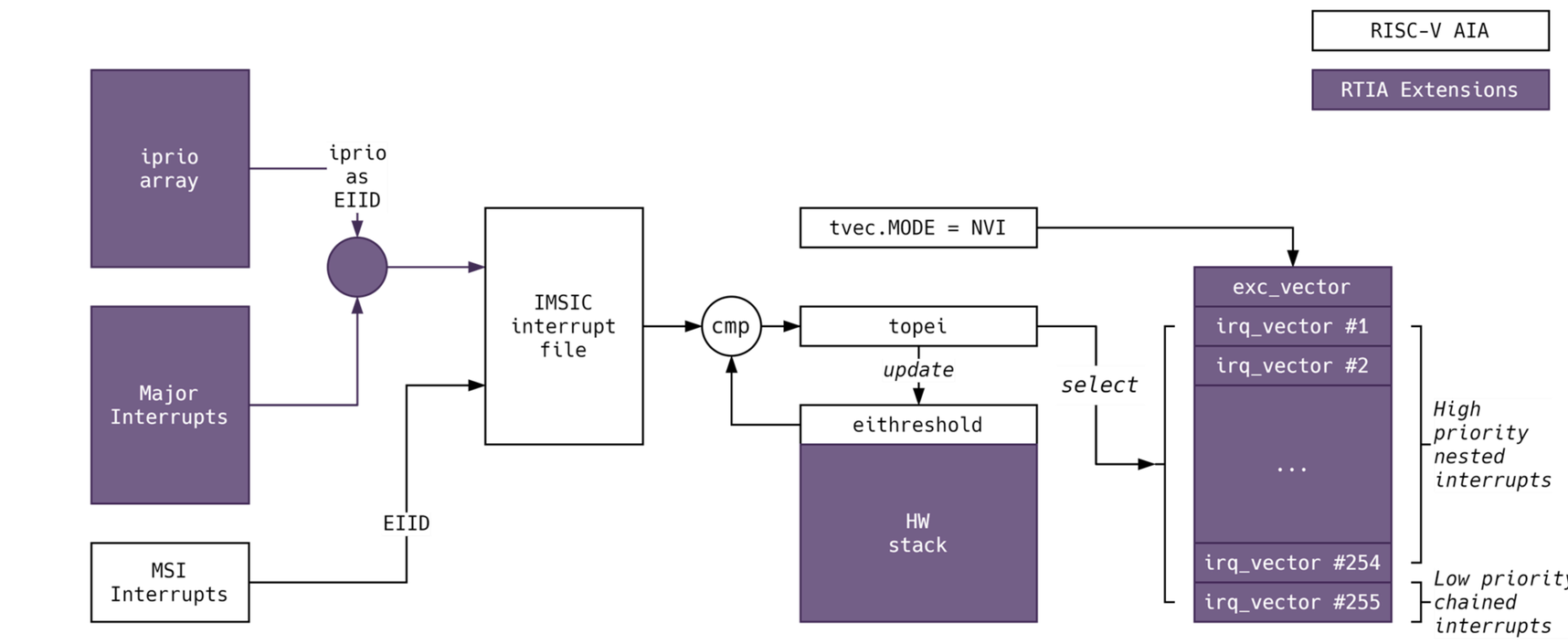
- Nested vectored interrupts
- Low latency interrupt delivery
- Light weight real-time interrupt architecture

Trap Stack Pointer Management



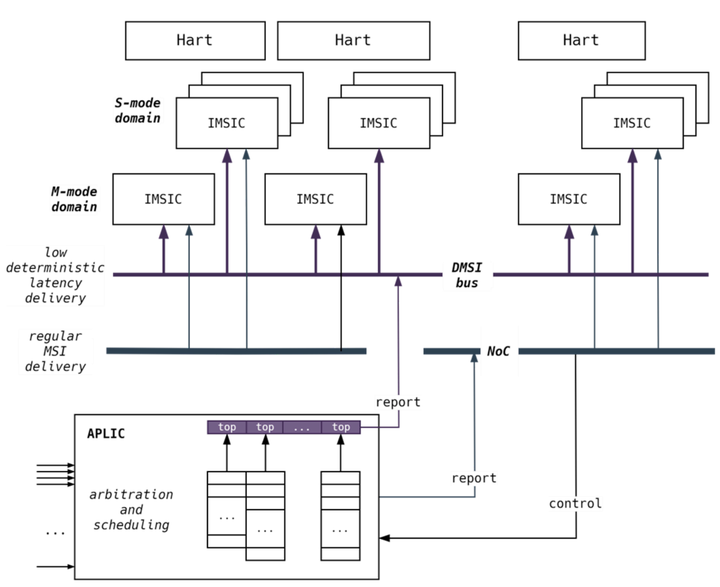
- Avoid stack-less execution in trap handler
- Reduce context store/restore overhead
- Allow hardware to automate trap frame
- Run-time configurable for each privilege mode
- Compatible with standard interrupt handling modes - *Direct*, *Vectored*

Nested Vectored Interrupts



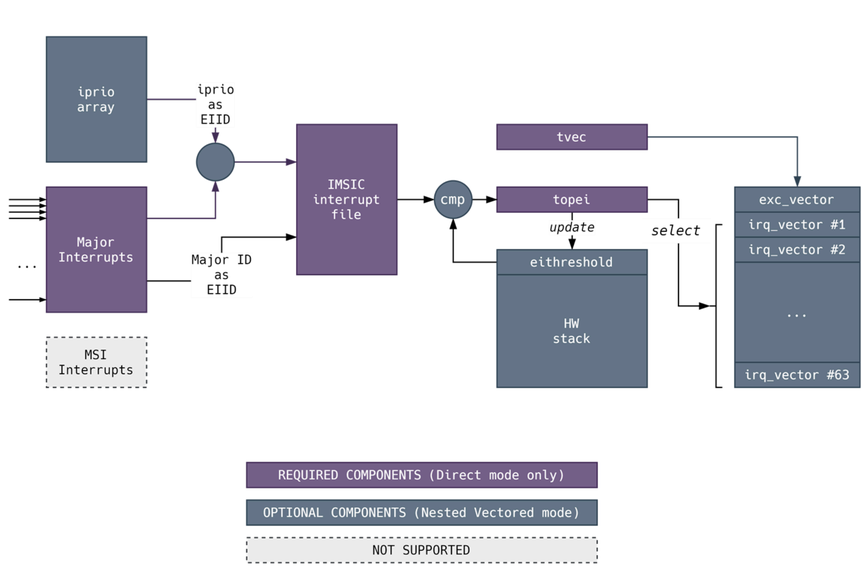
- New *Nested Vectored* interrupt handling mode
- Major interrupt reporting via IMSIC file (use *iprio* as EIID)
- External interrupt vectors table:
  - Single shared exception trap vector
  - Up to 255 high priority nested interrupts
  - Lower priority chained interrupts (share single vector)
- Automatic external interrupt claim and jump by vector
- Interrupt complete triggered from software
- Interrupt priority level threshold update at claim/complete

Real-Time Interrupt Delivery



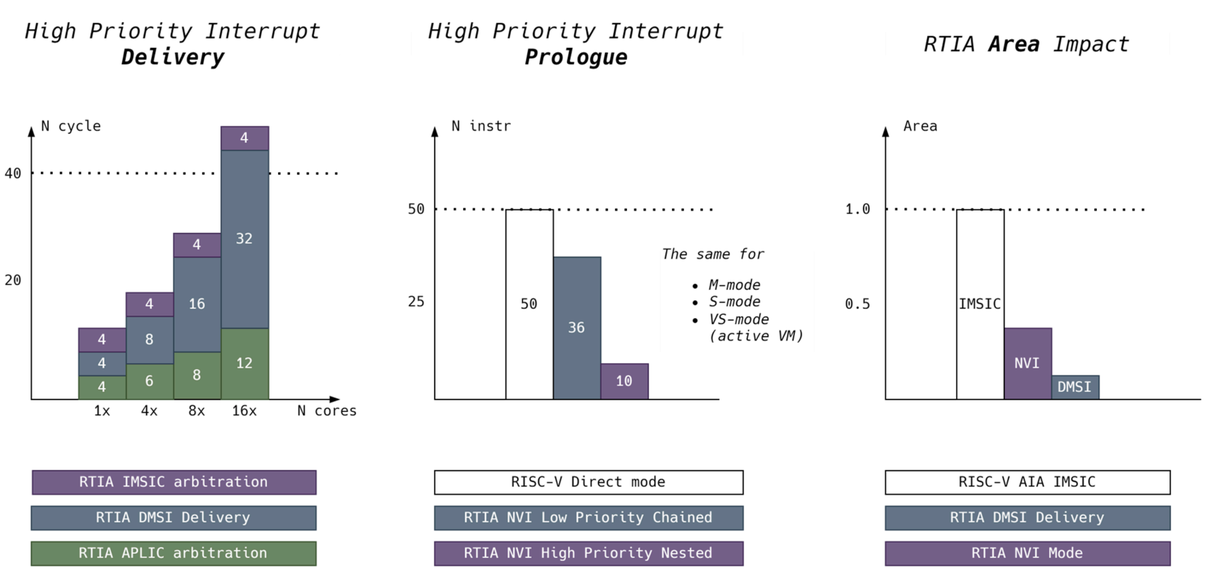
- New optional *Direct Message Signaling Interrupt* (DMSI) delivery mode
- Configurable for each interrupt source at APLIC side
- Wide bandwidth, deterministic low latency DMSI bus
- Delivery prioritization by domain, target, priority
- DMSI cannot be initiated in software, regular MSI can be used for IPI

Light Weight Real-Time Interrupt Architecture



- Core major interrupts routed via M-mode IMSIC file
- Fixed or configurable major interrupt priorities (*iprio* array) are used as IMSIC EIIDs
- Optional interrupt threshold and *Nested Vectored* interrupt handling mode with up to 63 priority levels
- Backward compatibility with RISC-V Privileged ISA and AIA

Latency and Area Impact



RTIA Extensions Development Status

Completed

- Synopsys RTIA Specification
- Functional simulator
- Functional tests
- Compiler support
- Synopsys ARC-V core IP (M/S/U-mode, no virtualization) RTL

In progress

- Synopsys ARC-V core IP (incl. H-extension) RTL
- Virtualization software prototype (Type-1) hypervisor
- RTIA support for Linux kernel
- OSS RTOSes porting

Plans

- RISC-V RTIA Specification Proposal