RISC-V MPU - Address Space Isolation for Latency Critical and/or Resource Constrained Systems

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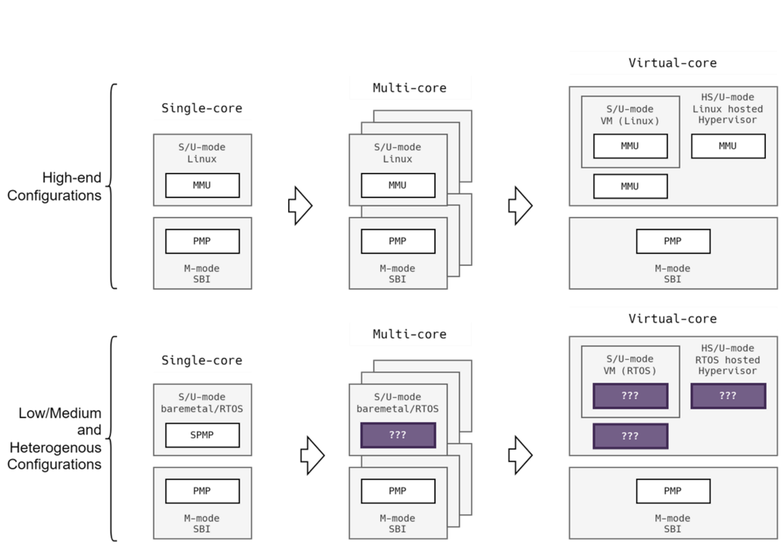
Motivation



MMU

- Paged virtual memory
- Flexible mapping
- Large configuration in memory
- Unpredictable latency

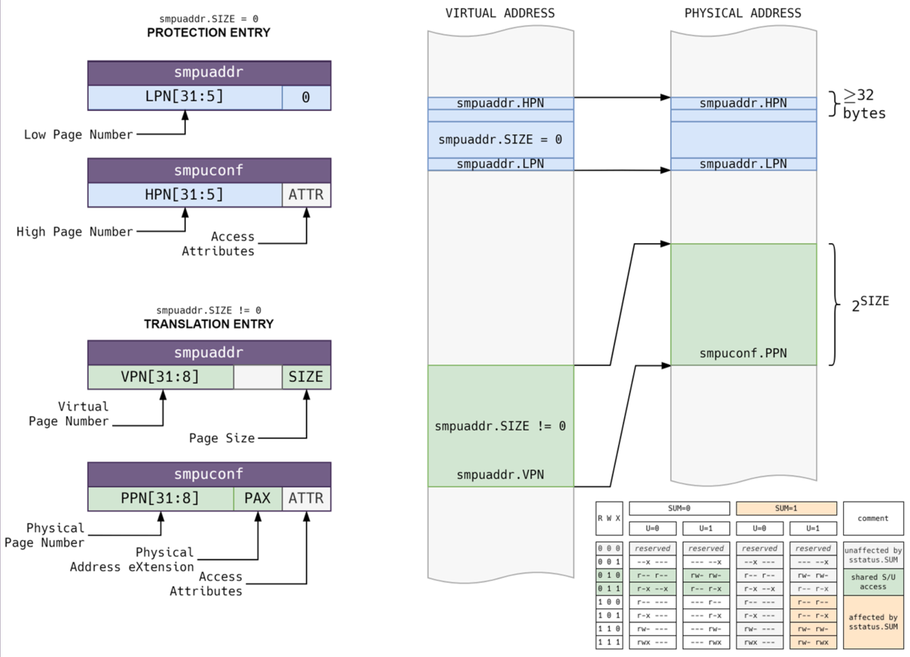
MPU

Combined fine grain address protection and deterministic low latency address translation

PMP

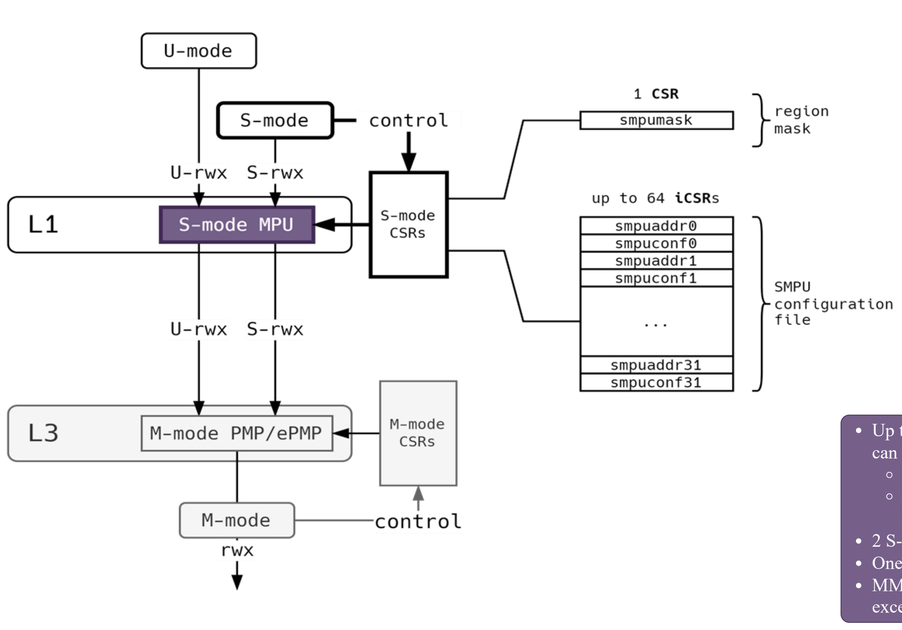
- Fine grain address protection
- Predictable latency
- Only physical addresses
- Inefficient multi-stage operation

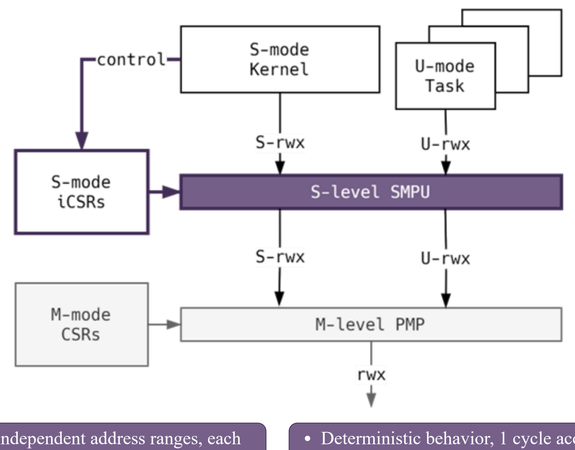
Unified Address Range Configuration

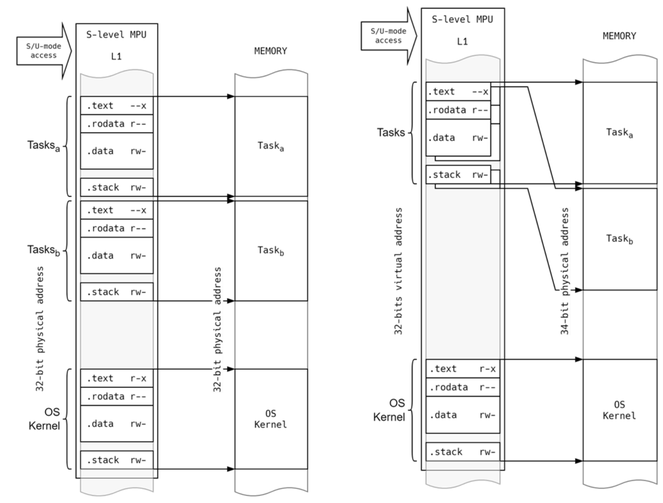


- Two iCSRs per address range:
  - **Protected Region** defined by base and limit address, or
  - **Translated Page** defined by VPN, PPN and SIZE
- Design-time adjustable protected region granularity
- Run-time configurable translated page size
- No priorities and/or dependencies across address regions
- Safe atomic run-time configuration update
- MMU compatible memory access attributes
- 32 -> 34-bit address extension (RV32)

S-level SMPU



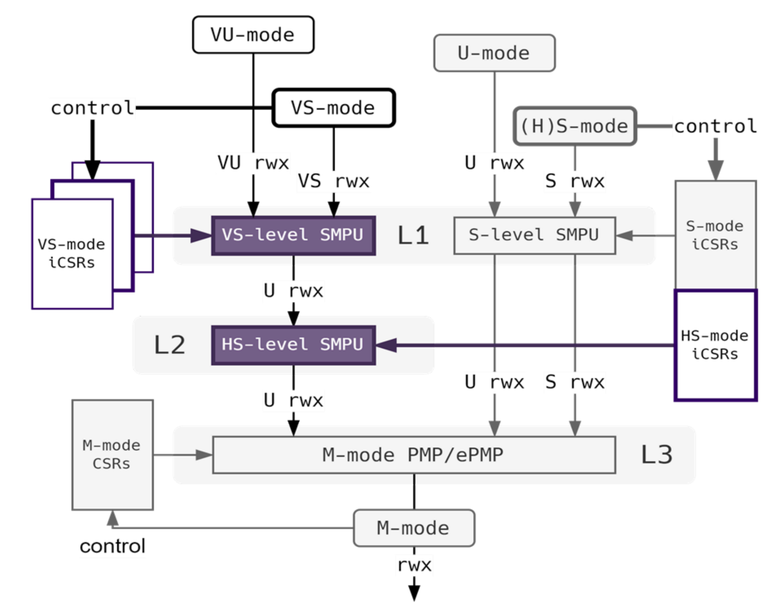


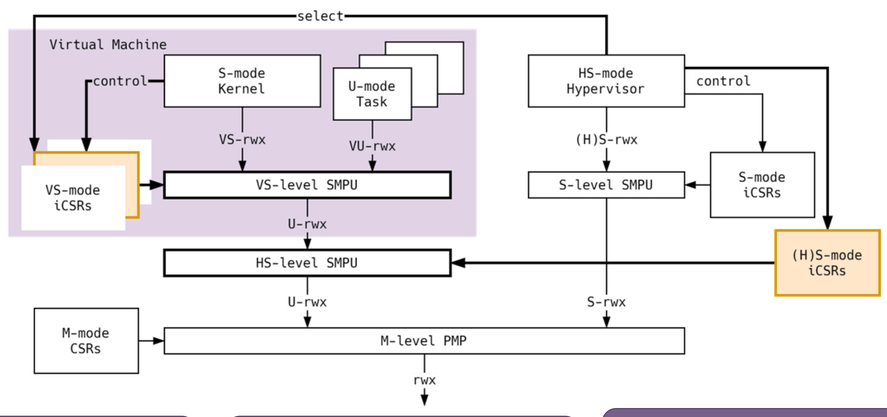


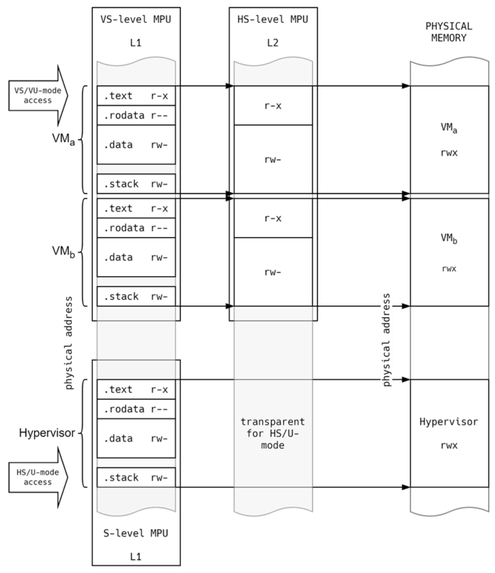
- Up to 32 (RV32) independent address ranges, each can be configured as:
  - Protected Region (min granularity 32 bytes), or
  - (optional) NAPOT Translated Page (min size 256 bytes)
- 2 S-mode iCSRs per region configuration
- One S-mode CSR with address range enable bit mask
- MMU style URWX access permssion encoding and exception traps

- Deterministic behavior, 1 cycle access latency
- Low overhead safe run-time configuration update
- Multiple programming models supported
- Multiple approaches to address map construction:
  - Static physical (supervisor/user isolation)
  - Dynamic physical (RTOS tasks isolation)
  - Static virtual (unified user process map)
  - Dynamic virtual (MMU emulation)
  - Combinations of all above

SMPU Hypervisor Extension







Two Stages Address Isolation and (optional) Translation

- All SMPU features are available in virtual environment (incl. optional translation)
- The same interface and programming model for all SMPU levels
- Simple cross-level SMPU configuration merge

RISC-V ISA Compliance

- Inherits RISC-V AIA component virtualization approach
- Compatible with RISC-V ISA H-extension, incl. extended instructions
- Compatible with paged memory (MMU), incl. advanced virtualization methodologies and unified VM address map

Flexible Design Options

- Flexible configuration options and extensions for wide range of applications
- Allows various hardware implementations with different performance/area goals
- Simplified integration with MMU-based high-performance cores and advanced system components (IOMMU)

Development Status

- RISC-V S-mode MPU Architecture Specification draft is available
- Software ecosystem
  - Simulation software with all features supported
  - Functional verification tests in progress
  - Real-Time Operating System prototype
  - Virtualization software (Type I hypervisor) prototype
  - virtIO subsystem in progress
  - OSS porting in progress
- Hardware implementation
  - RTL implementation in progress
  - RTL simulation in progress