RISC-V system prototyping in the RISER project

Manolis Marazakis

Institute of Computer Science, Foundation for Research and Technology – Hellas (FORTH), Greece

Abstract

Can we design and build data-center system platforms based on open standards in Europe today? This poster outlines the experiences and roadmap of an ongoing research and innovation project that has taken up this challenge. RISER (started in Jan'23) is progressing towards a first-generation of all-European RISC-V cloud accelerator and cloud server stand-alone prototypes, operating with fully-featured operating systems and runtimes. Building on top of outcomes from the EPI and EUPILOT projects, RISER aims to develop the first all-European RISC-V cloud server infrastructure, aiming to enhance Europe's open strategic autonomy. This poster summarizes the progress of prototyping effort by the project consortium.

Motivation & Background

The development and long-term evolution of general-purpose and accelerator processors, together with their associated set of hardware and systems software support components, has been widely recognized as a crucial element of open strategic autonomy for Europe. The European Cloud and Edge computing markets are projected to experience substantial growth, with an estimated increase from $56.85 billion to $470.13 billion between 2022 and 2032, for the cloud market and from $15.54 billion in 2023 to $147.38 billion by 2032 for the edge computing market, reflecting a compound annual growth rate (CAGR) of more than 25% [1]. Expanding and validating open hardware interfaces, coupled with making available a fully-featured operating system environment and runtime system, enables a pathway of innovation in several domains, including cloud services which are so widely adopted that they have become an essential part of everyday life. The concerns outlined above led to the conceptualization of the RISER project [2]. RISER aims to develop the first all-European RISC-V cloud server infrastructure, significantly enhancing Europe's strategic autonomy in open-source system technologies.

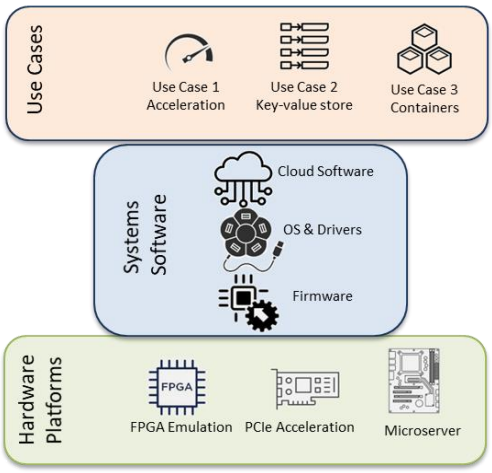

Figure 1 : RISER hardware platforms, system software & firmware, use cases.

Project Overview

The RISER project brings together seven partners from industry and academia to jointly develop and validate open-source designs for standardized form-factor system platforms, suitable for supporting cloud services. RISER is building two cloud-focused platforms:
(1) An accelerator platform, which includes an Arm SoC (from the EPI project [3]) at the host side and a PCIe acceleration board that integrates RISC-V vector-processor chips (from the EUPILOT project [4]).
(2) A microserver platform, interconnecting microserver boards to be developed by the project, each one with a RISC-V chip coupled with high-speed storage and networking. The open-source system board designs of RISER will be accompanied by open-source low-level firmware and systems software, and a representative Linux-based software stack to support cloud services, facilitating uptake and enhancing the commercialization path of project results. Figure 1 summarizes the main outcomes (hardware platforms and their associated firmware and system software support) planned in the RISER project. Three use cases are being developed:
(1) Acceleration of compute workloads;
(2) Networked object and key-value storage;
(3) Containerized execution as part of a provider-managed IaaS environment.

Prototyping Status

This poster illustrates the progress towards RISER's main outcomes, namely the development of prototypes of accelerator devices and microservers using RISC-V chips. The photographs arrayed in Figure 2 are snapshots of the development effort so far. We have built a FPGA-assisted prototype of the RISER accelerator card that runs a fully-fledged Linux distribution and operates in conjunction with a Linux-based host server. Ongoing effort is focused on (i) standalone operation (i.e. without any dependency with the host), and (ii) support for multi-device acceleration.

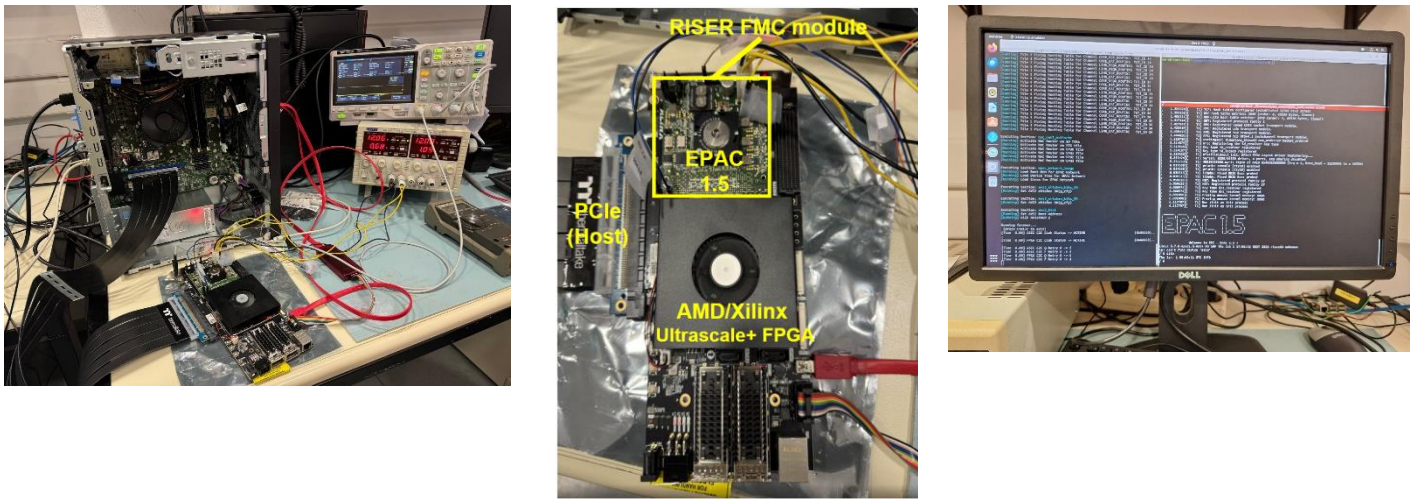

Figure 2 : Laboratory prototype of RISER accelerator card (running Linux). The prototype uses the EPAC1.5 test-chip from the EPI project.

Acknowledgements

The RISER consortium is comprised of the following partners:

1. **FORTH (Greece):** Firmware & System SW, Project coordination
2. **EXAPSYS (Greece):** HW prototyping, PCBs & assembly
3. **SEMIDYNAMICS (Spain):** Verification, FPGA-based emulation
4. **BSC (Spain):** Use Cases and Evaluation, Open Access
5. **SIPEARL (France):** Requirements, PCI accelerator, Dissemination/Communication
6. **EXTOLL (Germany):** Architecture & Specifications, High-speed links
7. **CLOUDSIGMA (Switzerland – Associated partner):** Dissemination, Exploitation, Evaluation.

RISER has received funding from the European Union's Horizon Europe research and innovation programme under grant agreement no. 101092993. The project is funded under the European Health and Digital Executive Agency (HaDEA) call on "Digital and emerging technologies for competitiveness and fit for the green deal".

References

[1] https://finance.yahoo.com/news/edge-computing-market-size-best-175948424.html
[2] RISER Project: https://riser-project.eu
[3] EPI Project: https://www.european-processor-initiative.eu/
[4] EUPILOT Project: https://eupilot.eu