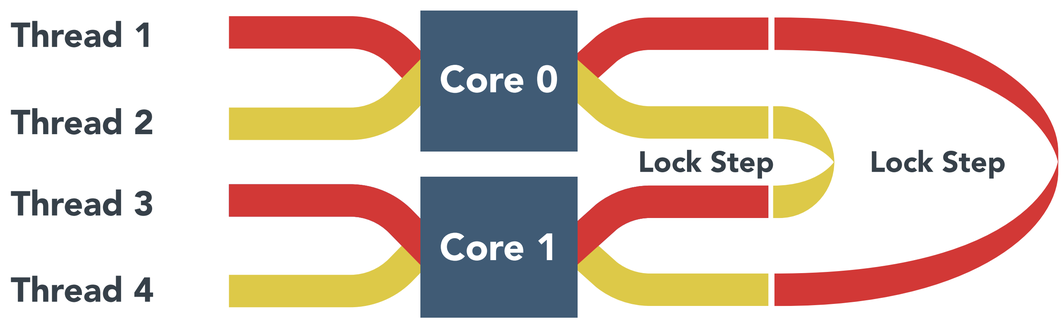
ECARX | ASIL D Automotive-Certified RISC-V Processor

High Safety | Automotive-Grade Certification | Secure Cryptographic Solutions

› Interleaved Two-thread Design

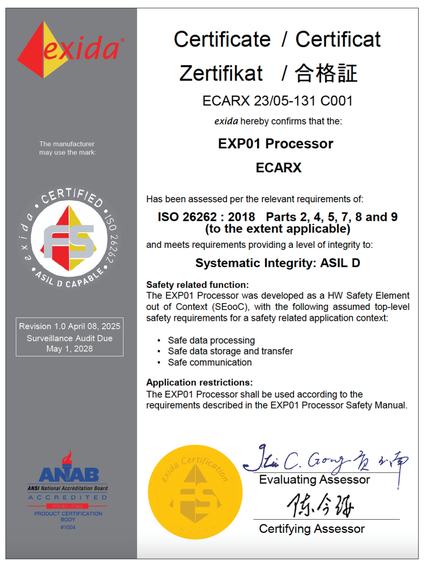
- Dual-core Lockstep (ASIL-D Compliant)
- 1.3x Higher Performance Efficiency
- 27% Silicon Area Reduction
- Optimized I-cache & D-cache to Avoid Thrashing



Instruction 1 (0)	IA	IF	ID	EX	WB					
Instruction 1 (1)		IA	IF	ID	EX	WB				
R5=R6*R7 (0)			IA	IF	ID	EX	WB			
JAL JALR (1)				IA	IF	ID	EX	WB		
R4=R4+R5 (0)					IA	IF	ID	EX	WB	
Instruction 3 (1)						IA	IF	ID	EX	WB

Thread (0) Thread (1)

› Automotive SoC Product Tape-out



exida

The manufacturer may use the mark:

CERTIFIED ISO 26262 ASIL D CAPABLE exida

Revision 1.0 April 08, 2025
Surveillance Audit Due May 1, 2026

ANAB ACCREDITED PRODUCT CERTIFICATION BODY #1004

Certificate / Certificat
Zertifikat / 合格証

ECARX 23/05-131 C001

exida hereby confirms that the:

EXP01 Processor

ECARX

Has been assessed per the relevant requirements of:

ISO 26262 : 2018 Parts 2, 4, 5, 7, 8 and 9 (to the extent applicable)

and meets requirements providing a level of integrity to:

Systematic Integrity: ASIL D

Safety related function:
The EXP01 Processor was developed as a HW Safety Element out of Context (SEooC), with the following assumed top-level safety requirements for a safety related application context:

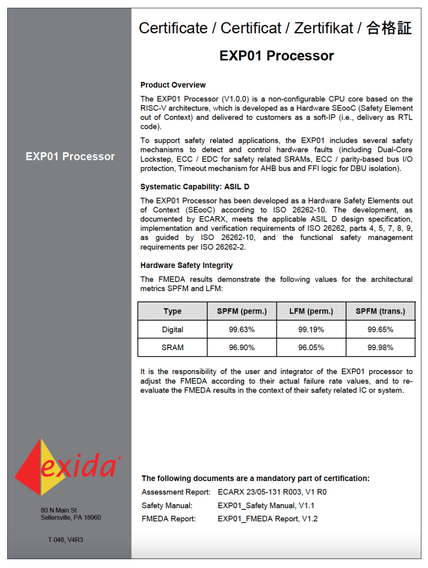
- Safe data processing
- Safe data storage and transfer
- Safe communication

Application restrictions:
The EXP01 Processor shall be used according to the requirements described in the EXP01 Processor Safety Manual.

exida Certification

Evaluating Assessor

Certifying Assessor



EXP01 Processor

exida

80 N Main St
Sellersville, PA 18960

T-048, V4R3

Certificate / Certificat / Zertifikat / 合格証

EXP01 Processor

Product Overview

The EXP01 Processor (V1.0.0) is a non-configurable CPU core based on the RISC-V architecture, which is developed as a Hardware SEooC (Safety Element out of Context) and delivered to customers as a soft-IP (i.e., delivery as RTL code).

To support safety related applications, the EXP01 includes several safety mechanisms to detect and control hardware faults (including Dual-Core Lockstep, ECC / EDC for safety related SRAMs, ECC / parity-based bus I/O protection, Timeout mechanism for AHB bus and FFI logic for DBU isolation).

Systematic Capability: ASIL D

The EXP01 Processor has been developed as a Hardware Safety Elements out of Context (SEooC) according to ISO 26262-10. The development, as documented by ECARX, meets the applicable ASIL D design specification, implementation and verification requirements of ISO 26262, parts 4, 5, 7, 8, 9, as guided by ISO 26262-10, and the functional safety management requirements per ISO 26262-2.

Hardware Safety Integrity

The FMEDA results demonstrate the following values for the architectural metrics SPFM and LFM:

Type	SPFM (perm.)	LFM (perm.)	SPFM (trans.)
Digital	99.63%	99.19%	99.65%
SRAM	96.90%	96.05%	99.98%

It is the responsibility of the user and integrator of the EXP01 processor to adjust the FMEDA according to their actual failure rate values, and to re-evaluate the FMEDA results in the context of their safety related IC or system.

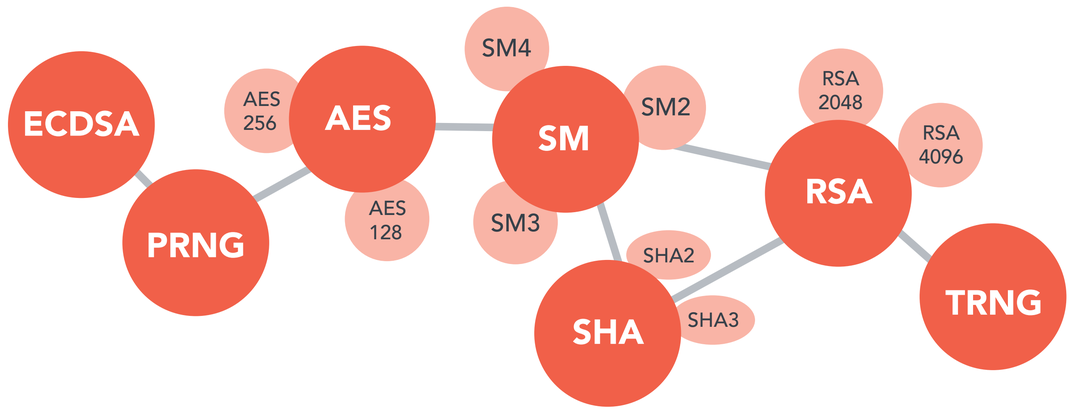
The following documents are a mandatory part of certification:

Assessment Report: ECARX 23/05-131 R003, V1 R0
Safety Manual: EXP01_Safety Manual, V1.1
FMEDA Report: EXP01_FMEDA Report, V1.2

› Presented at RISC-V Summit CHINA 2024

RISC-V Based Crypto – HSM:

- RISC-V (eCore)
- Vector Crypto Extension
- Custom Instruction



	SHA2-256	ECDSA-256	AES128
Our Results	239 MB/s	143 times/s	247 MB/s
Available Main-Stream Solution	98 MB/s	100 times/s	14 MB/s
	Vendor A	Vendor B	Vendor C

› ECARX RISC-V IP Cores

Ecore
RISC-V 32IMC
Embedded
Shadow RegFile

Ccore
RISC-V 32x
Computing-Core
High Performance

Acore
RISC-V 32IMFCA
Application Processor
Supervisor/User Mode with Memory Protection

Rcore
RISC-V 32EMC
Area Reduction for MACE

Xcore
RISC-V 64
Linux, Hypervisor

www.ecarxgroup.com
For any inquiries regarding the poster content, please contact: lei6.shi@ecarxgroup.com; mei2.wang@ecarxgroup.com