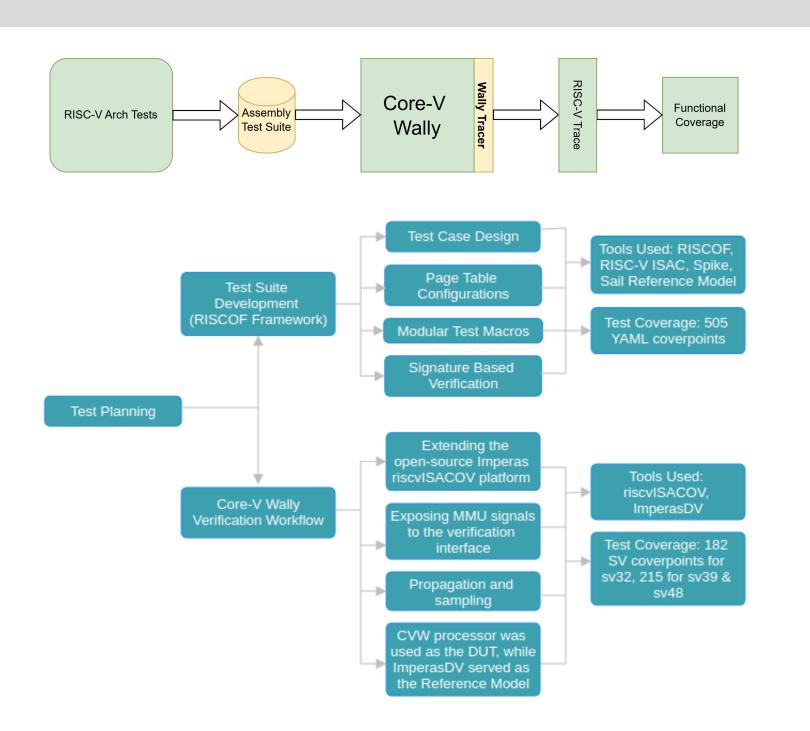
Comprehensive Verification of the RISC-V Memory Management Unit: Challenges and Solutions

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Introduction

The Memory Management Unit (MMU) enables virtual address translation, memory protection, and multitasking. Ensuring compliance with the RISC-V Privileged ISA is crucial for interoperability. However, its configurability—supporting multiple paging schemes and superpage translations—poses significant verification challenges, especially in open-source cores where edge cases and ambiguities can cause critical flaws.



Test Planning

- Unified DV Plan for all MMU configurations
- Key Verification Areas:
 - PTE Permission Bits Tested across all page table levels in supervisor & user modes.
 - Global Mappings & satp Register Ensures correct address translation and ASID

Results/Findings

This work was implemented and validated on Core-V Wally, a 5-stage pipelined processor supporting configurations from RV32E to a full RV64GC application processor. The proposed test suite successfully uncovered a critical bug in the MMU through the reserved_pte_s_mode test. The bug caused Core-V Wally to fail in triggering a page fault when accessing memory regions mapped by Page Table Entries (PTEs) with reserved RWX encoding (pte.W=1 and pte.R=0), violating the RISC-V Privileged ISA specification.

- handling.
- Virtualization in Machine Mode
- TVM Bit Functionality
- Supervisor Access to U-Mode Pages
- MXR (Make eXecutable Readable)

Conclusion

- Enhanced verification framework for RISC-V MMUs
- Discovered a major flaw in Core-V Wally's MMU implementation
- Improved compliance testing for open-source processor designs
 Our methodology strengthens MMU
 validation for open-source RISC-V cores, ensuring better reliability and compliance.

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