RISC-V®

The RISE Project: Advancing RISC-V Software

Ludovic Henry, RISE TSC
Nathan Egge, RISE TSC

May 2025

Mobilizing Software Ecosystem for Growth

Collaboration & Community Engagement

Investing in the Software Stack Fundamentals

Continuous Software Porting and Optimization

Collaboration: RISE (RISC-V Software Ecosystem)

Raise

RISC-V platform quality

Ensure

RISC-V is tier 1 for tools and libraries

Align

Ecosystem partners efforts for adoption

How: Working Upstream, Transparently

Open and Transparent Organization

Coordinating contributions

Bringing open source communities together

RISE Members

Premier Members

ANDES TECHNOLOGY

Google

達摩院 DAMO ACADEMY

Imagination

intel

MEDIATEK

NVIDIA

Qualcomm

Red Hat

Rivos

SAMSUNG

SiFive

VENTANA

General Members

AKEANA

AMD

BOSC 北京开源芯片研究院 BEIJING INSTITUTE OF OPEN SOURCE CHIP

ByteDance

Canonical

ESWIN 奕斯伟计算

ISCAS 中国科学院软件研究所 Institute of Software Chinese Academy of Sciences

MICROCHIP

SPACEMIT 进迭时空

tenstorrent

ZTE

Additional Information: https://riseproject.dev/

RISE Software Focus Areas

Coordination and collaboration among the RISE members is across an array of software areas to deliver high quality and high performance implementations for RISC-V software

Compilers & Toolchains	LLVM, GCC, GLIBC
System Libraries	FFmpeg, OpenBLAS, oneDAL, XNNPACK, oneDNN
Kernel & Virtualization	Linux, Android
Language Runtimes	Python, Java/OpenJDK, Go, JavaScript/V8, WebAssembly, Rust, .NET
Linux Distro Integration	Ubuntu, Debian, RedHat, Fedora, Alpine, RockyLinux, AlmaLinux, Gentoo
Debug & Profiling Tools	Performance Profiles, DynamoRIO, Valgrind
Simulators/Emulators	QEMU, SPIKE
System Firmware	UEFI, U-Boot, Coreboot, TF-M
Developer Infrastructure	Build Farm, Board Farm, Developer Tools
Security Software	Secure Root-of-Trust, Confidential Compute
AI/Machine Learning	PyTorch, TensorFlow, TFLite, Llama.cpp

Check out the RISE Wiki: https://wiki.riseproject.dev/

NEW

AI/ML Working Group

Open source accelerates AI development and ensures a transparent RISC-V ecosystem

RISE AI/ML Working Group drives collaboration on PyTorch, TensorFlow, TFLite and Llama.cpp

Enhancing AI software performance strengthens RISC-V's position as a competitive AI Platform

Recent RFPs Focus on:

Optimization of PyTorch, OpenBLAS, and oneDNN for RISC-V

llama.cpp Progress Sharing
128-bit RVV in K-Quant Kernels

Xiongchuan Tan
April 23, 2025

Develop and upstream a high-performance RVV 1.0 port of Llama.cpp

RFP Highlighted Results

☑ LLVM SPEC optimization

Reduces execution time by 15% on SPEC CPU® 2017-based benchmark on SpacemiT-X60
Improved Vectorization Efficiency, better Register Allocation, and more work to be done

☑ Go

Compiler Optimization: expanding RVV and bitmanip support, implementing math and crypto intrinsics
Releases available since Go 1.21 at https://go.dev/dl

☑ Python Packaging

Building packages for commonly used projects
https://gitlab.com/riseproject/python/

☑ QEMU TCG

Enhanced performance for vector (V) and crypto (Zvk) extensions; faster emulation and CI/CD. Achieved 2x faster memory operations and halved AOSP boot time.

☑ Rust

On track to meet full Tier-1 requirements

☑ OpenOCD

RISC-V support upstreaming

☑ LLVM CI

Leveraged QEMU-based testing to support profiles and optimized build configurations.

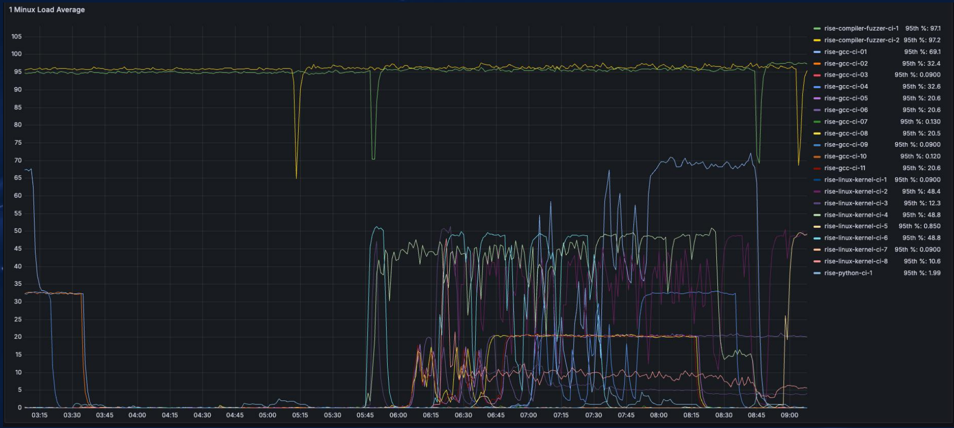
Developer Infrastructure

Build Farm

- Integration to Kernel and GCC CI: more testing to improve quality
- Increase quality while landing large autovectorization changes in GCC with pre-commit and post-commit automated testing
  - 137 bugs found and fixed with fuzzing
  - 792 post-commit builds, 400+ patches tested pre-commit
  - Fixing compiler bugs affecting SPEC

Board Farm

- Some usage of Scaleway EM-RV1
- Partnership with Eclipse Adoptium
  - Released Java 17, 21, 23 and later



Developer Appreciation Program

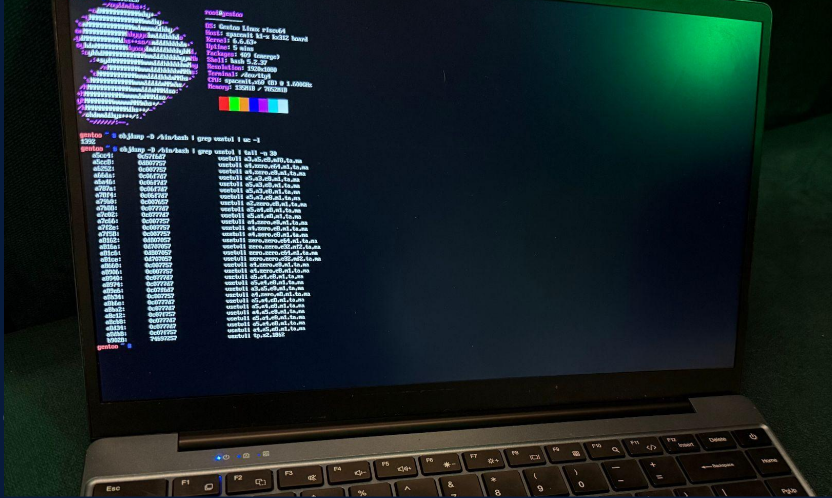
Rewarding Developers who port Software to RISC-V

- 500€ for Small contributions, 3000€ for Large contributions
- File an issue: https://github.com/rise-dev-appreciation

Rewarded contributions

- Gem5 - Support for H Extension and SVNAPOT - #5 #12
- Delve - A Go debugger - #8
- VOLK 🌋 - Vector-Optimized library used by GNU Radio project - #11
- syscall_intercept - User-space interception of system calls - #9
- Lightening - Template based JIT library - #10
- SIMD Everywhere - Portable SIMD library - #4
- MAMBO - Dynamic binary instrumentation and modification - #3

Gentoo Developer Images



```
root@gentoo
-----------
OS: Gentoo Linux riscv64
Host: spacemit k1-x kx312 board
Kernel: 6.6.63+
Uptime: 5 mins
Packages: 409 (emerge)
Shell: bash 5.2.37
Resolution: 1920x1080
Terminal: /dev/tty4
CPU: spacemit,x60 (8) @ 1.600GHz
Memory: 135MiB / 7852MiB

gentoo ~ $ objdump -D /bin/bash | grep vsetvl | wc -l
1392
gentoo ~ $ objdump -D /bin/bash | grep vsetvl | tail -n 30
   a5cc4:       0c57f6d7                vsetvli a3,a5,e8,mf8,ta,ma
   a5cc8:       0d807757                vsetvli a4,zero,e64,m1,ta,ma
   a6252:       0c007757                vsetvli a4,zero,e8,m1,ta,ma
   a66da:       0c06f7d7                vsetvli a5,a3,e8,m1,ta,ma
   a6a46:       0c06f7d7                vsetvli a5,a3,e8,m1,ta,ma
   a787a:       0c06f7d7                vsetvli a5,a3,e8,m1,ta,ma
   a78f4:       0c06f7d7                vsetvli a5,a3,e8,m1,ta,ma
   a79b0:       0c007657                vsetvli a2,zero,e8,m1,ta,ma
   a7b88:       0c0777d7                vsetvli a5,a4,e8,m1,ta,ma
   a7c02:       0c0777d7                vsetvli a5,a4,e8,m1,ta,ma
   a7c66:       0c007757                vsetvli a4,zero,e8,m1,ta,ma
   a7f2e:       0c007757                vsetvli a4,zero,e8,m1,ta,ma
   a7f58:       0c007757                vsetvli a4,zero,e8,m1,ta,ma
   a8162:       0d807057                vsetvli zero,zero,e64,m1,ta,ma
   a816a:       0d707057                vsetvli zero,zero,e32,mf2,ta,ma
   a81c6:       0d807057                vsetvli zero,zero,e64,m1,ta,ma
   a81ce:       0d707057                vsetvli zero,zero,e32,mf2,ta,ma
   a8660:       0c007757                vsetvli a4,zero,e8,m1,ta,ma
   a8906:       0c007757                vsetvli a4,zero,e8,m1,ta,ma
   a8940:       0c0777d7                vsetvli a5,a4,e8,m1,ta,ma
   a8974:       0c0777d7                vsetvli a5,a4,e8,m1,ta,ma
   a89e6:       0c07f6d7                vsetvli a3,a5,e8,m1,ta,ma
   a8b34:       0c007757                vsetvli a4,zero,e8,m1,ta,ma
   a8b6e:       0c0777d7                vsetvli a5,a4,e8,m1,ta,ma
   a8ba2:       0c0777d7                vsetvli a5,a4,e8,m1,ta,ma
   a8c12:       0c07f757                vsetvli a4,a5,e8,m1,ta,ma
   a8cb8:       0c0777d7                vsetvli a5,a4,e8,m1,ta,ma
   a8d34:       0c0777d7                vsetvli a5,a4,e8,m1,ta,ma
   a8db8:       0c07f757                vsetvli a4,a5,e8,m1,ta,ma
   b9028:       74697257                vsetvli tp,s2,1862
gentoo ~ $
```

Project Goals

- Turn-key images to jump-start developers with latest toolchains:
  - gcc-15.1 clang-20.1.3 rust-1.86 glibc-2.41
- Produce images quickly for RVV hardware
  - Kernel + U-Boot + OpenSBI + 409 packages in **less than 5 hours**
- Bespoke CFLAGS for each devboard platform
  - Now building with -O3 -march=rv64_zvl256b
  - Surfaced and filed *many* GCC bugs 116242 [meta-bug] zvl issues in RISC-V
- Talk to us about adding your devboard!

[1] Canaan K230 https://people.videolan.org/~negge/canaan-3G-2024-04-08.img.xz

[2] BPI F3 / ROMA II https://dev.gentoo.org/~lu_zero/riscv/gentoo-linux-k1_dev-sdcard-2.1.0-20250411-rvv.img.xz

[3] Orange Pi RV2 https://people.videolan.org/~negge/gentoo-linux-x1_dev-sdcard-20250422-rvv.img.xz

Developer Resources

RISC-V Optimization Guide

- https://gitlab.com/riseproject/riscv-optimization-guide

RISE Case Study: Adding RVV 1.0 to dav1d AV1 decoder

- Part 1 - 2023-Oct-31, Part 2 - 2023-Nov-14, Part 3 - 2024-Mar-14
- RISCV-Summit EU 2024 Optimizing Software for RISC-V (slides)
- RISC-V 101 2024 (slides) RISC-V 101 2025 (slides)

Python Packaging

- https://gitlab.com/riseproject/python/
- 49 Python projects made available on RISC-V, and counting

How RISE is Contributing

- Foster Public Open Source Standard Collaboration
- Establish Developer Infrastructure
- Activate Broader Developer Community

How you can get involved

- Becoming a member
- Request For Proposals (RFPs)
- Developer Appreciation Program

Shared Vision for Future

Building Stronger RISC-V Software Ecosystem Together