EuroHPC
Joint Undertaking

From Open Silicon to Sovereign Supercomputing: EuroHPC's Vision for RISC-V

RISC-V Summit Europe

14th May 2025 | **Alexandra Kourfali** | Paris, FR

Who are we?

- EU body & legal and funding entity
- Created in 2018
- Autonomous since Sep. 2020
- Based in Luxembourg
- A team of 47+ employees
- Still growing!

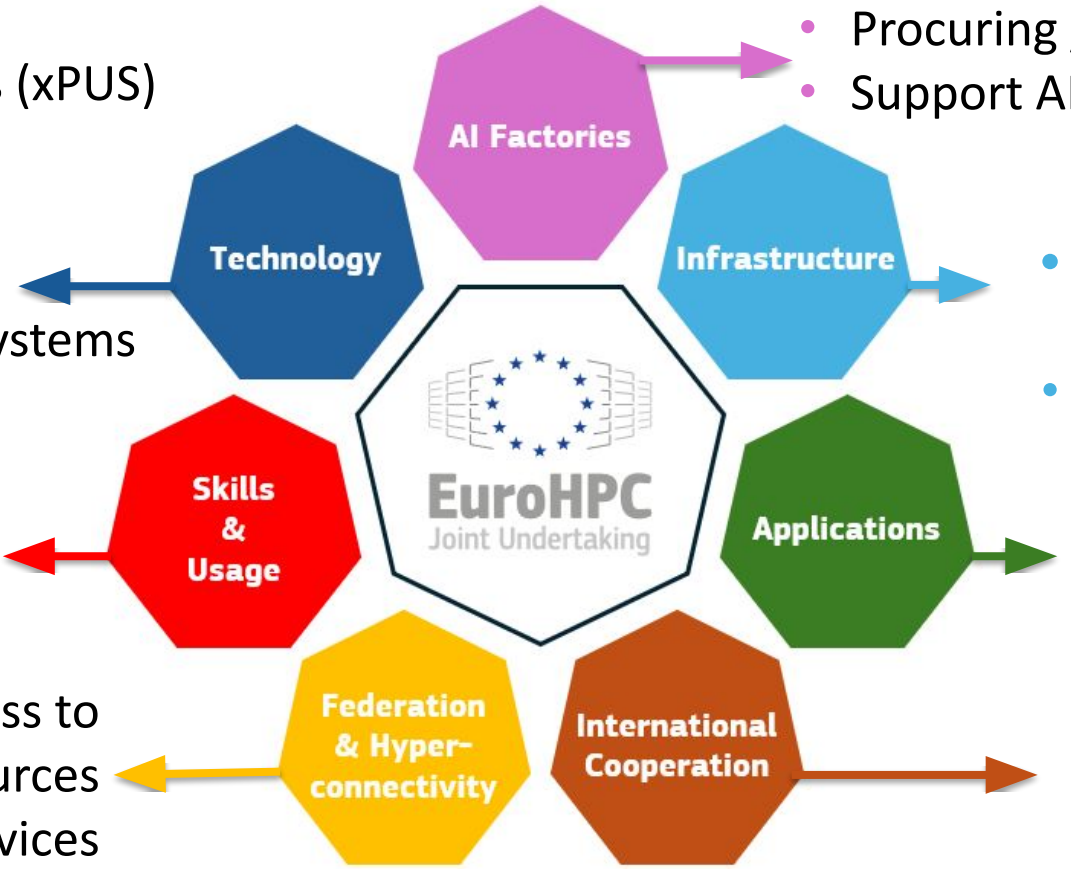
Our Mission

R&I activities to develop:

- **Hardware** components (xPUS)
- **Pilots**
- **Software** stack
- **Quantum** integration
- **Energy-efficient** HPC systems

- **Training** programmes to develop HPC skills base in Europe

- Development of access to **federated** HPC resources and services



- Procuring /upgrading **AI**-oriented **HPC systems**
- Support AI app development in EU

- **Procuring**/deploying HPC & QC SOTA systems
- Providing **access** to EU users

- Algorithms, SW development
- **Centers of Excellence**

Collaboration with **3rd countries**

- Solve global challenges
- Strengthen EU competitiveness

EuroHPC infrastructure

HPC Systems

3 PRE-EXASCALE

- Lumi, FI #5 TOP500
- Leonardo, IT #7
- Marenostrum 5, ES #8

5 PETASCALE

- Vega, SL
- Karolina, CZ
- Discoverer, BG
- Meluxina, LU
- Deucalion, PT

Ongoing

2 EXASCALE

- Jupiter, DE #1 Green500
- Alice Recoque, FR

Quantum

- **8 quantum computers**
- **2 quantum simulators**

Consortia of 30+ countries

AI Factories

EuroHPC supercomputers

- AI-ready
- AI-upgrades
- AI-optimized

Consortia of 21+ countries

13 EU sites selected

Our Organization

Co-funded by EU, Participating States and Private Members

The European Union
represented by the
European Commission

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3 Private Members

34 Participating States

Our Organization

Co-funded by EU, Participating States and Private Members

European Commission

Digital Europe
1.98 B€
- Infrastructure
- HPC services Federation
- Usage, skills

Horizon Europe
900 M€
- **Technology**
- Applications
- International Cooperation

Connecting Europe
200 M€
- Hyperconnectivity
- Data connectivity

EuroHPC Joint Undertaking

Total investments
7 B€ in 2021-2027

R&I
≈ 2 B€ in 2021-2027

900 M€
from 3 Private Members

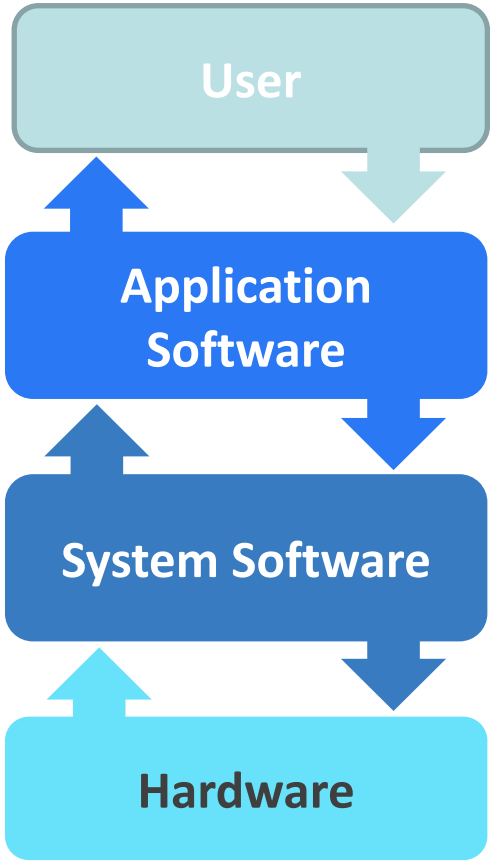
3 B€ from
34 Participating States

Currently around **40 R&I projects** on **technology, applications & skills**

Strategic Research & Innovation areas

EuroHPC JU funds an R&I programme to develop a full **European supercomputing ecosystem,** support European **digital autonomy,** to reduce Europe's dependency on **foreign manufacturers**

- **Leadership in Use & Skills**
  Competence Centres & training programmes in HPC commensurate with the labour market.
- **Applications and Algorithms**
  Centres of Excellence for HPC Applications & algorithms for EU exascale
- **European Software Stack**
  SW, algorithms, programming models and tools for exascale & post exascale
- **European Hardware**
  Ecosystem for low power high-end general purpose processor & accelerator



HPC microprocessor technology: Strategy

EU goal: autonomy in strategic processing technologies

DESIGN

Short term (2025-27)

Medium term (2028-30)

Long term (2030-)

First IPs

- **Build on EPI** efforts
- From test chips to **TRL 9**
- RISC-V processors and accelerators: chiplets, advanced nodes
- EuroHPC exascale systems as first customer

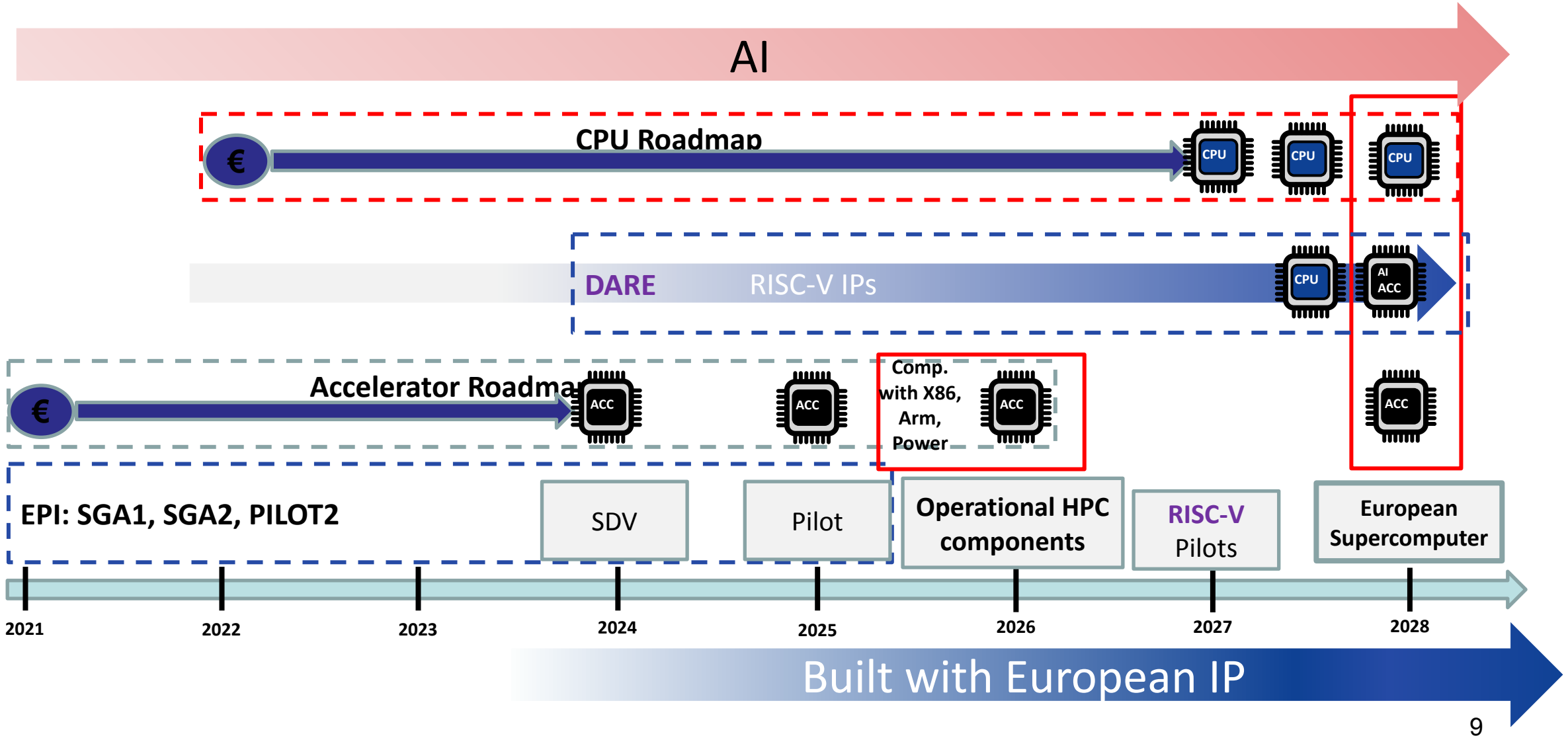
New RISC-V architectures complement the work of EPI and DARE

- Pilots on RISC-V with stand-alone competitive xPUs
- Collective effort building on **EU R&D** in low power, AI, security,…,
- EuroHPC **post-exascale** system as first customer

Post-exascale RISC-V systems based on EU R&D

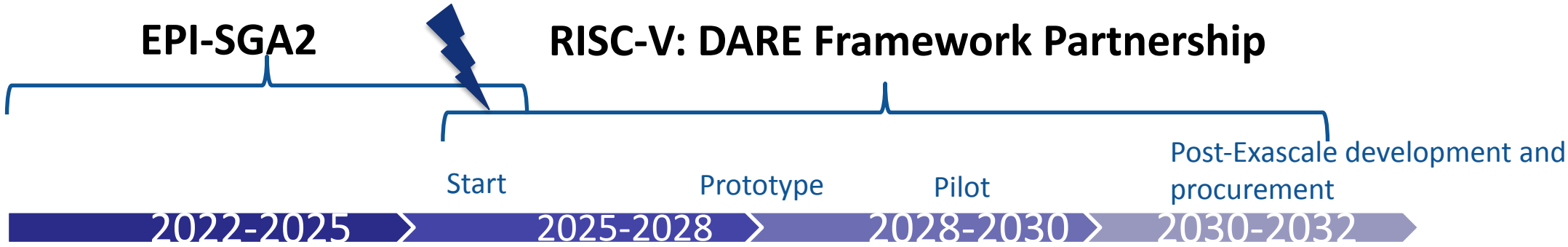
- **RISC-V ISA plays a central role on EU's technology strategy**
- ***AI needs are reforming EU's strategy in processors***

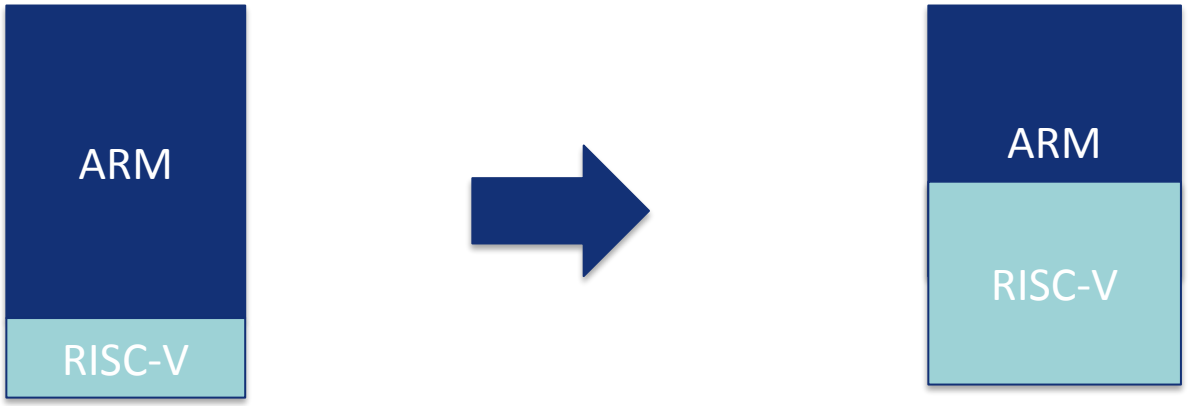
EuroHPC Chips Roadmap



HPC microprocessor technology

State of play

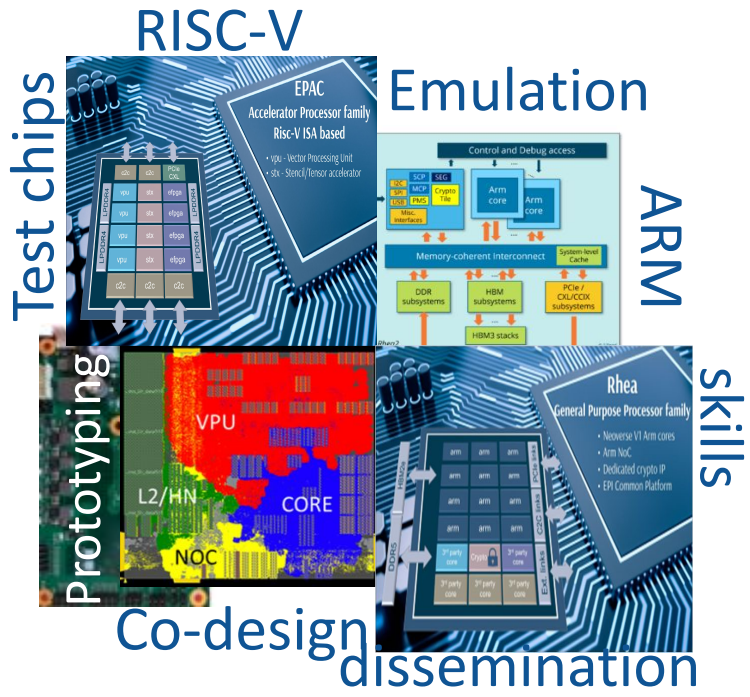




- EPI: European low-power microprocessor technologies
- DARE: Large-scale European initiative for High Performance Computing ecosystem based on RISC-V

European Processor Initiative at EuroHPC

EPI umbrella and ecosystem



European Processor Initiative at EuroHPC

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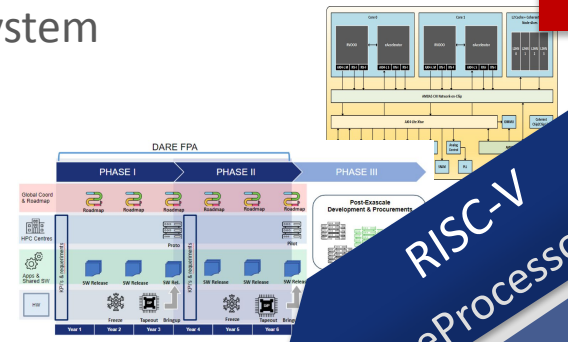
EPI umbrella and ecosystem

8 M€

240 M€



RISC-V
DARE, eProcessor, …

RHEA family

RISC-V

Test chips

Emulation

ARM

EPAC
Accelerator Processor family
Risc-V ISA based

EPI

150 M€

Prototyping

skills

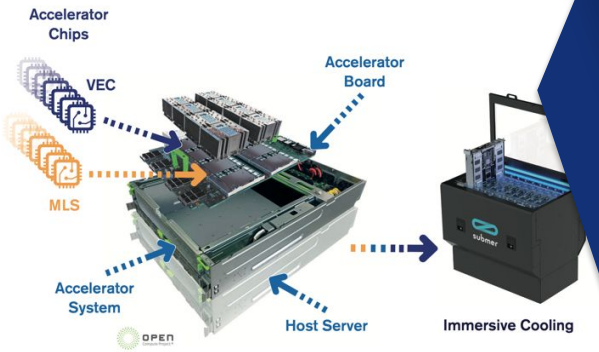
EUPILOT

EUPEX

Co-design

dissemination

40 M€



30 M€

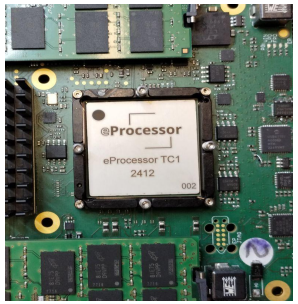
RISC-V chips development status

EPI

- EPAC 1.5 (2nd gen)
- SDV

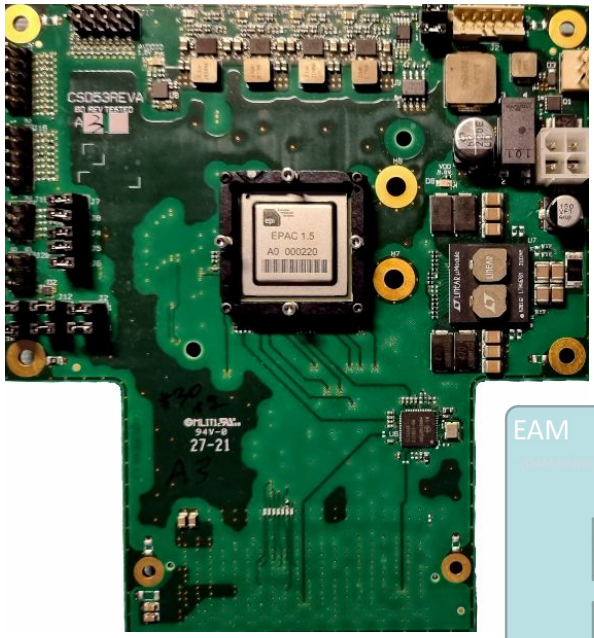
EUPILOT

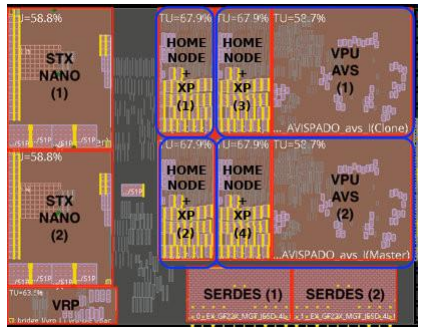
- VEC: Global Foundries 22 nm
- Next GEN:
  - VEC : 59 mm² GF 12nm
  - MLS : 20 mm² TSMC 7nm

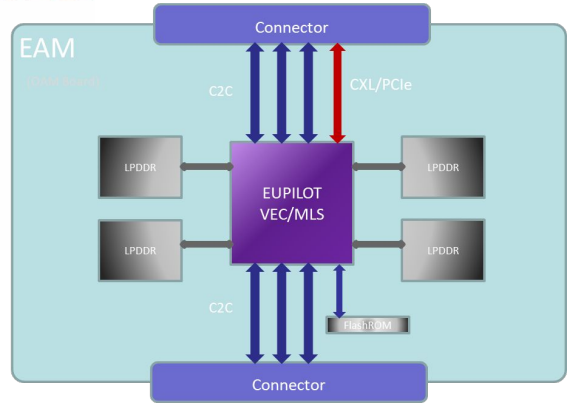


eProcessor

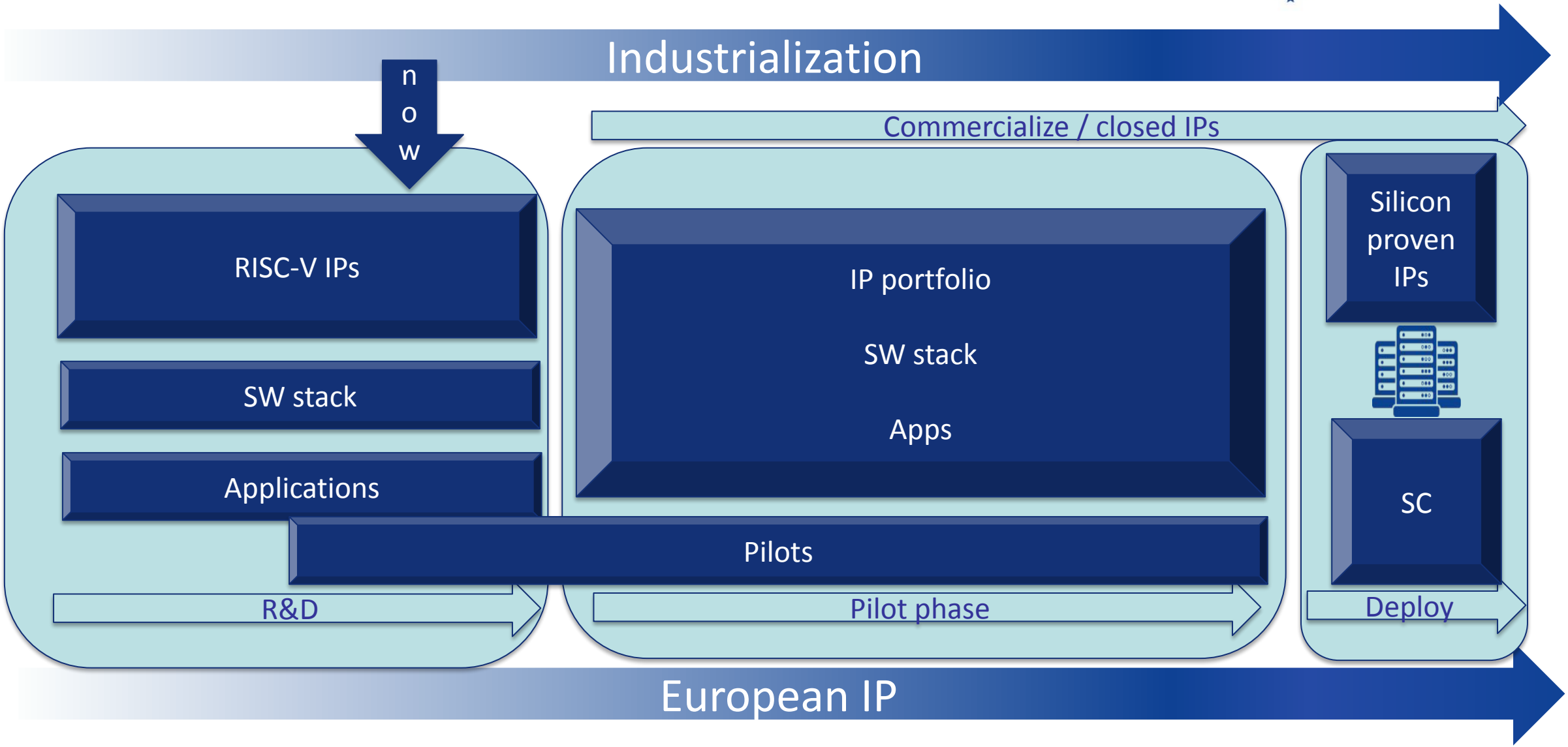
- 1 RVOOO core, 1 eAccelerator, 2 L2 slices
- GF 22nm, 10.40 mm²



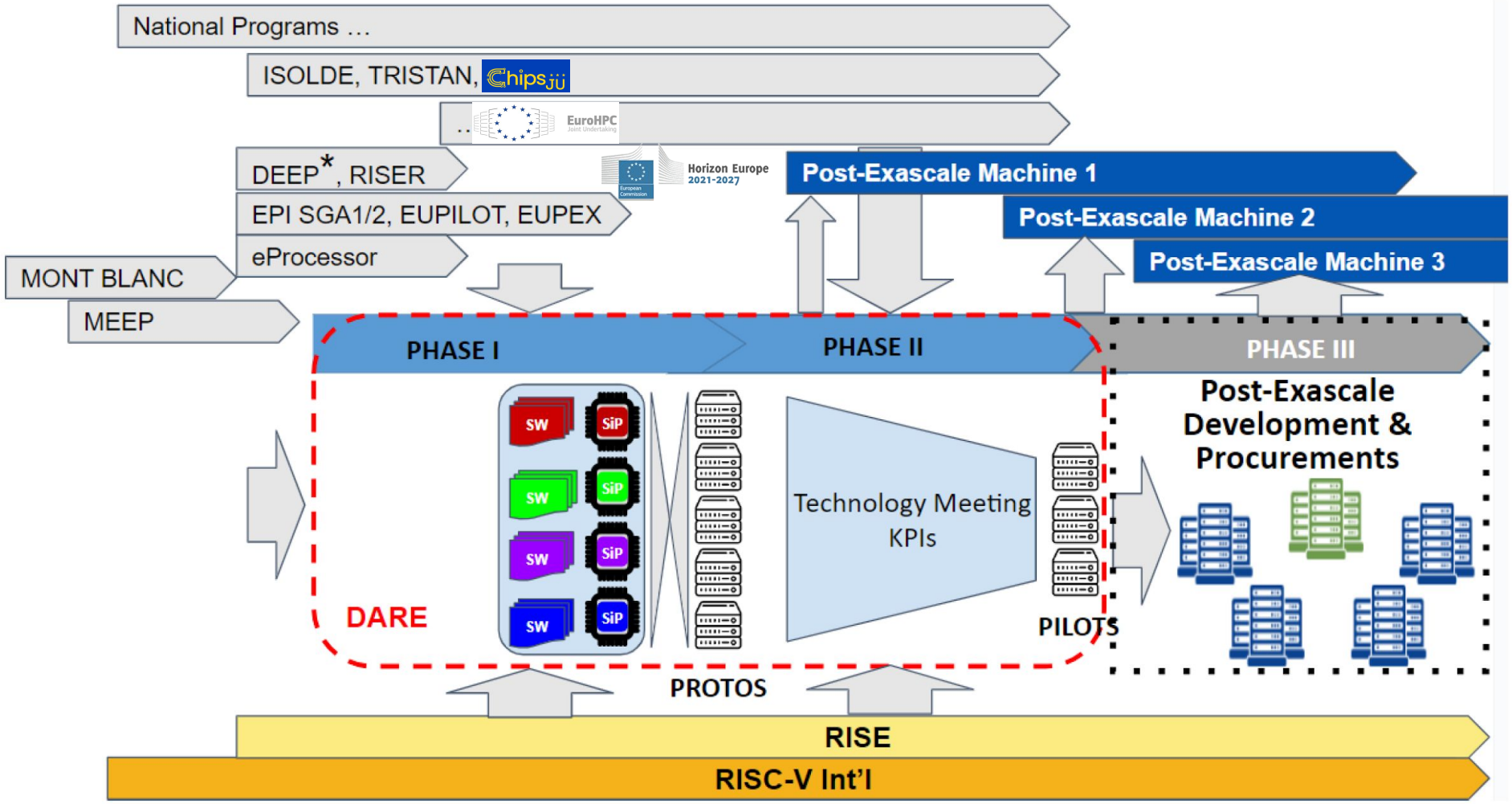




RISC-V Roadmap



Digital Autonomy with RISC-V in Europe



dare Roadmap for EuroHPC RISC-V

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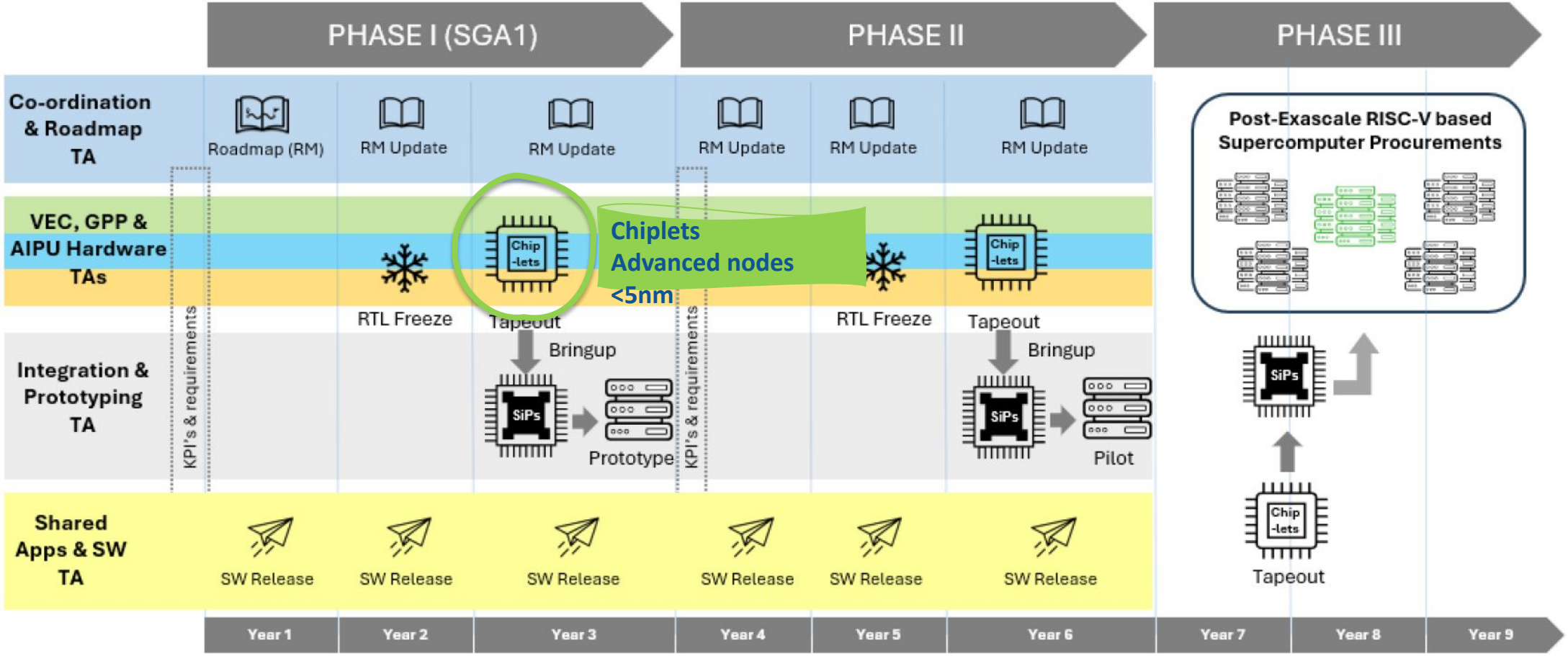


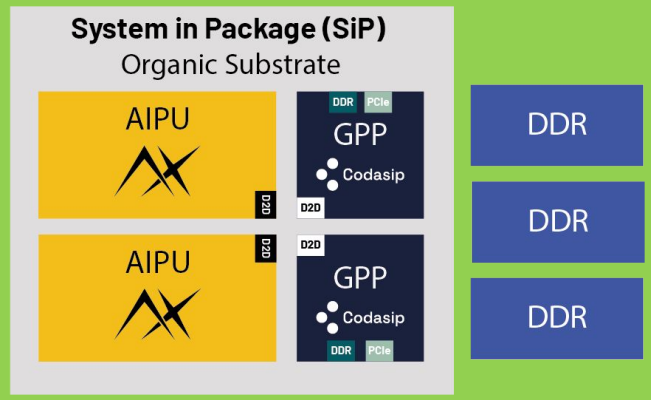
DARE Technical Areas

BSC Coordination
(Roadmap, Technical Coordination, PMO, Diss & Inn)

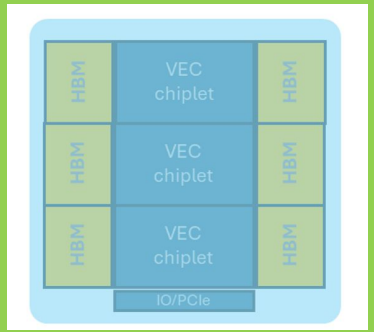
JSC & BSC Shared Software

Axelera: AI Inference Accelerator

CODASIP: GPP

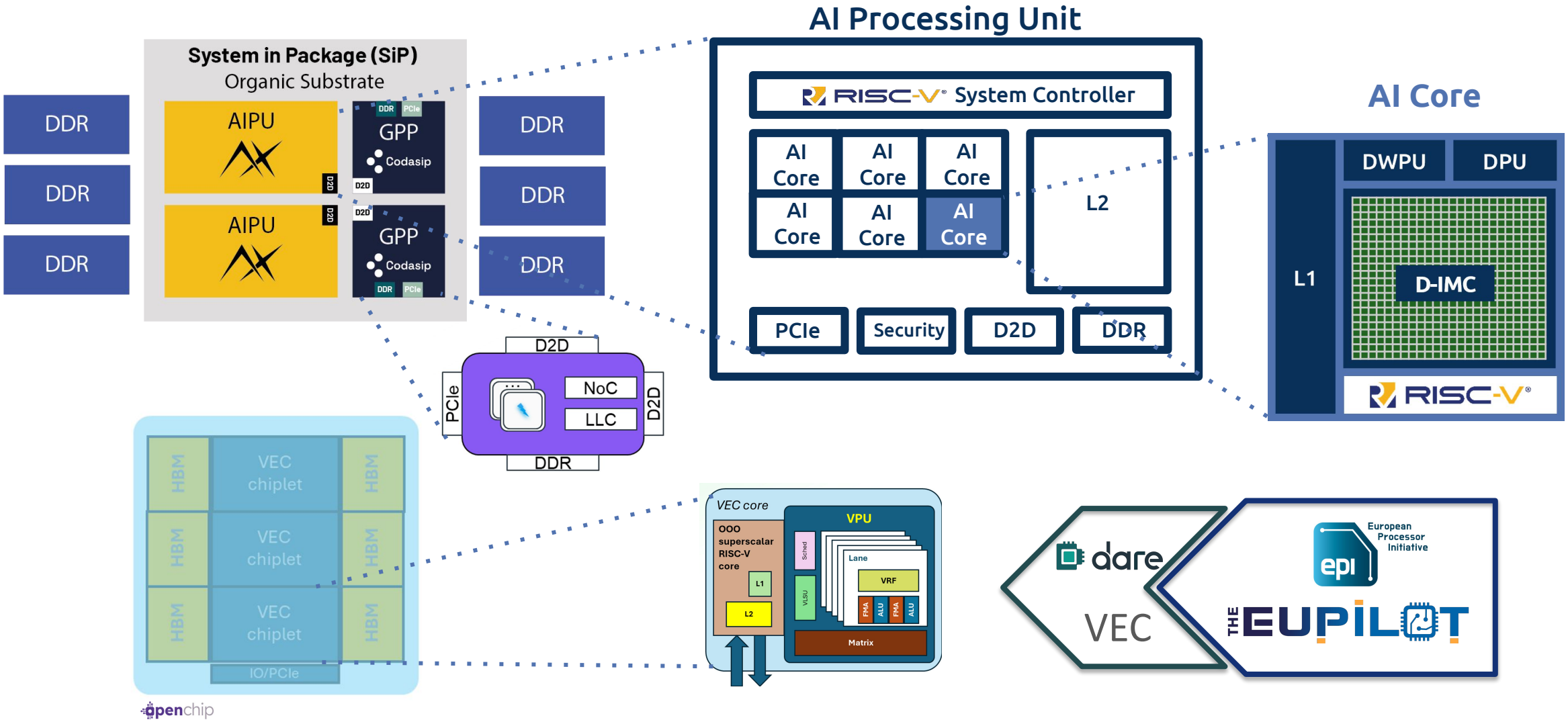


Openchip
Vector Accelerator

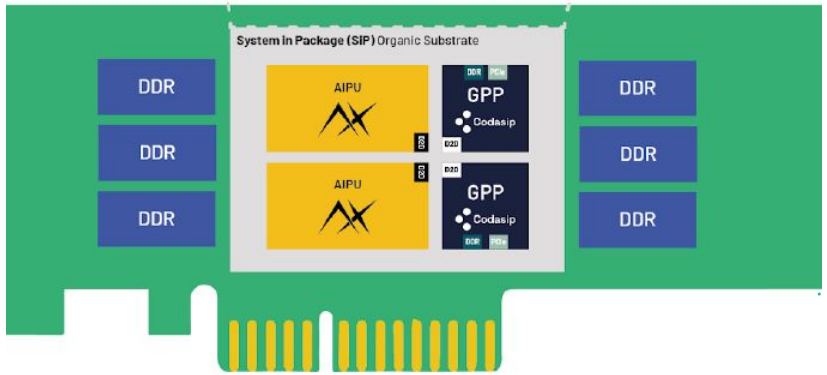


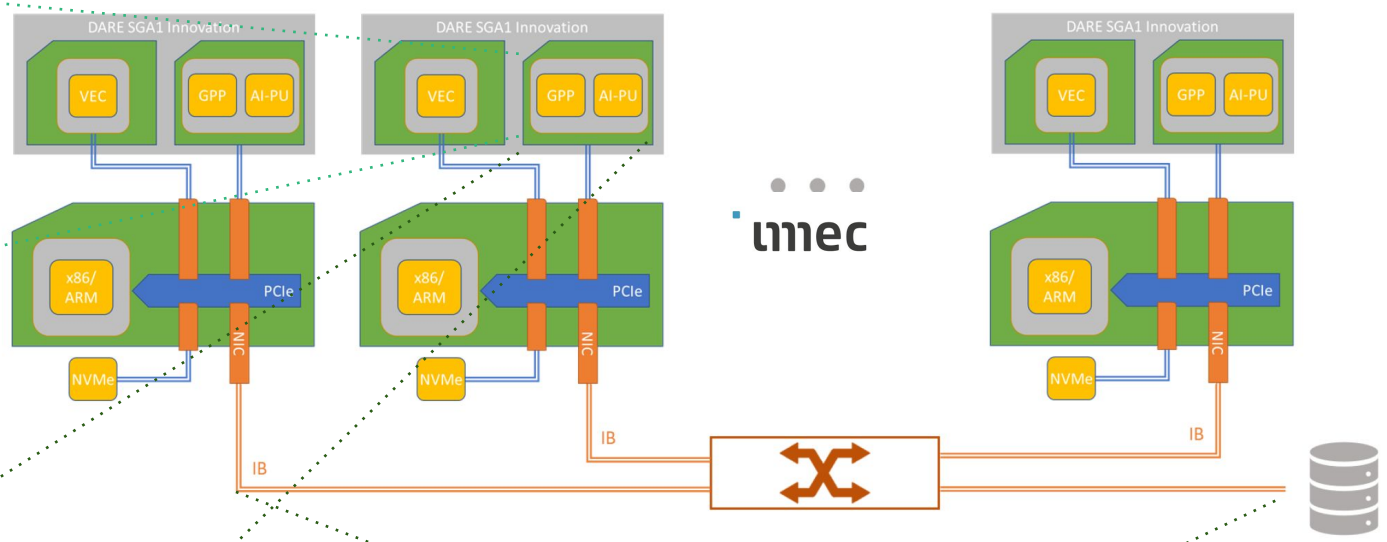
IMEC packaging, testing

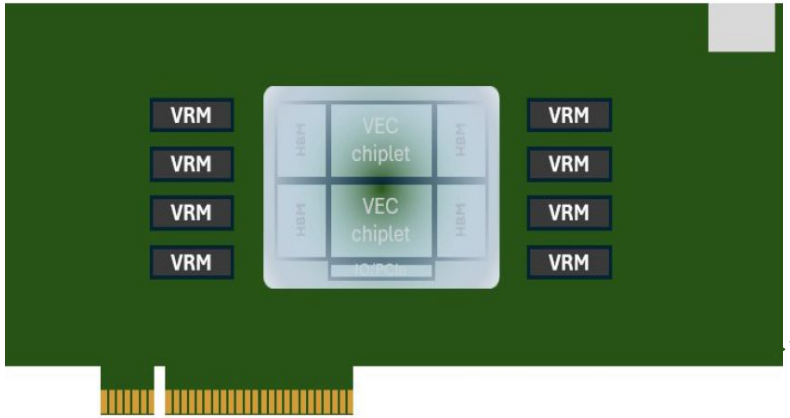
DARE Technical Areas : Chiplets

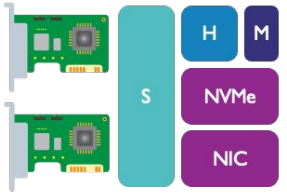


DARE Technical Areas : Integration



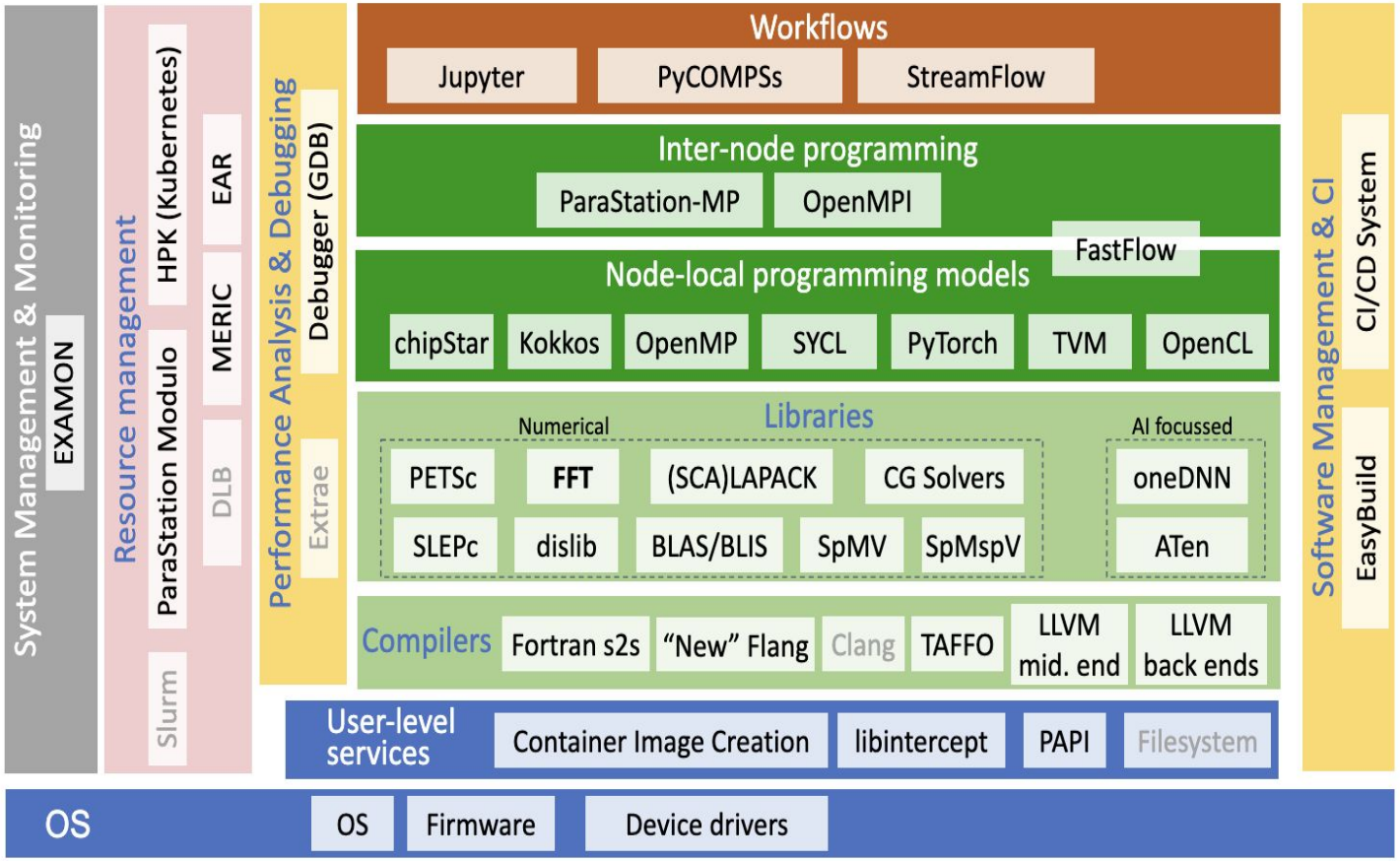






Machine ~ 1000 Nodes	Server ~ 2x-4x Nodes	Node = Host + Devices
Machine = 128x-256x Racks Rack = 8x-16x Servers Network Switches Network Topologies	Multi-Node (2x-4x) Standard Server Config. Network Switches Network Topologies	Host (x86) + Memory PCIe Cards (Devices) Switch (PCIe → CXL) Storage (NVMe)

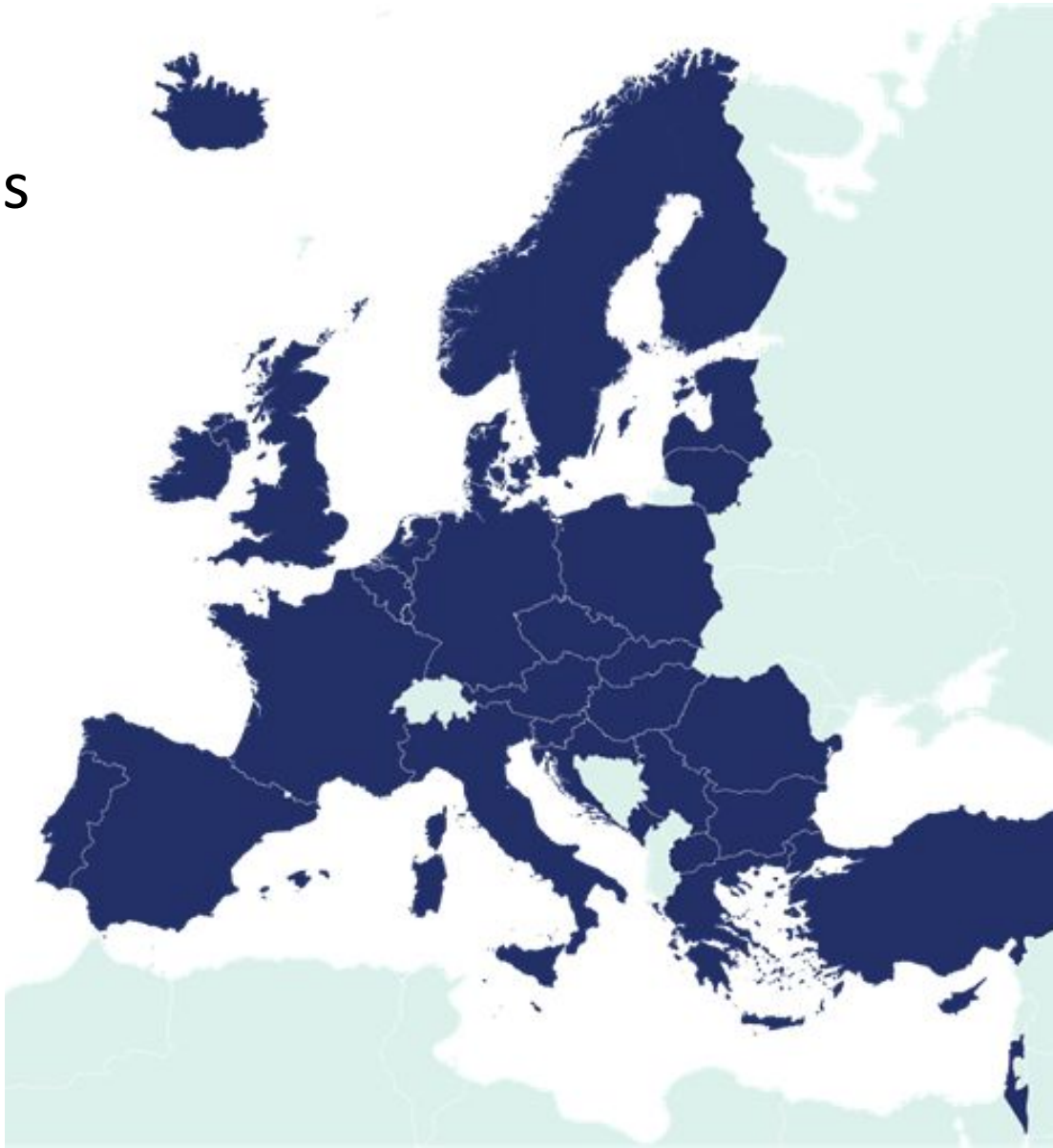
DARE Technical Areas : SW Stack



- Integrated and optimized **SW stack**
- Based on **existing standards**
  - MPI, OpenMP, Fortran, BLAS, SYCL, PyTorch, …
- Focus on
  - Compilers, especially Fortran
  - Autovectorization and OpenMP
  - Optimized libraries for HPC, AI
  - MPI
- Build on **EU strengths** in HPC & AI
  - Optimize applications and SW stack for DARE chiplets
- HW/SW **co-design**
- Contribute to **Open-Source** SW RISC-V implementations
- Leverage RISC-V **SDVs**

Conclusions

- RISC-V is **inevitable**!
  - **Inclusiveness** in participating in actions from academia and industry
  - **Cutting edge** technology, chiplets and advanced nodes
- **SW stack** is crucial
  - One of the most critical parts
- **Consolidated** effort of projects
  - develop tech diversity
- Clear, ambitious **vision** & roadmap



The European High Performance Computing Joint Undertaking

LEADING THE WAY IN EUROPEAN SUPERCOMPUTING

May 2025 | **Alexandra Kourfali**

THANK YOU

EuroHPC
Joint Undertaking

For more information, feel free to visit our website and social media:

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