# Flex-RV: World's First Non-silicon RISC-V Microprocessor*

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## Abstract

*We present, Flex-RV, a 32-bit microprocessor based on RISC-V instruction set fabricated with Indium-Gallium-Zinc-Oxide (IGZO) thin-film transistors (TFTs) on a flexible substrate, enabling an ultra-low-cost bendable microprocessor, which makes the World's first non-silicon RISC-V microprocessor. Flex-RV integrates a programmable machine learning (ML) hardware accelerator, and demonstrates new instructions to extend the RISC-V instruction set to run ML workloads. It is implemented, fabricated and demonstrated to operate at 60 kHz consuming less than 6 mW power and its functionality when assembled onto a flexible printed circuit board is validated whilst executing programs under flat and tight bending conditions. Flex-RV pioneers an era of ultra low-cost open standard non-silicon 32-bit microprocessors for applications at Extreme Edge.*

## Introduction

There is a new class of emerging applications that require embedded electronics not only being capable of sensing, computing, communicating at low cost and power but also providing qualitative features such as form factor, conformability (i.e., taking the shape and contour of the surface), user comfort and biocompatibility. We categorize these emerging applications as applications at the **Extreme Edge** [2]. Some examples of Extreme Edge applications are fast-moving consumer goods (e.g., smart labels and packaging in drink bottles, food packages, personal care products etc.), healthcare wearables (e.g., smart patches, dressings, neural interfaces), and healthcare teststrips (e.g., lateral flow tests, microfluidics), smart textiles (e.g., garments and carpets) and agritech (e.g., plant monitoring).

A computing system for Extreme Edge applications is composed of low-cost electronic components fabricated on flexible substrates (e.g., printed sensors, printed batteries/energy harvesters, e-paper displays and a microprocessor) to offer the qualitative features. The computational requirements of Extreme Edge applications are not demanding in terms of performance as they are mainly sensor-driven applications where sensor data sampling times are in the range of milliseconds to even minutes [3][4].

Traditional silicon-based solutions, while powerful and efficient, face some hurdles to meet quantitative (e.g., cost) and almost all qualitative features required by Extreme Edge applications. To overcome these hurdles, we must explore new materials and simpler architectures that can offer flexibility, ultra-low cost, thin form factor and seamless integration with our environment, all while providing the necessary computational power for embedded machine learning. Thus, we introduce Flex-RV [1] (**Figure 1**) — the first programmable and "bendable" general-purpose 32-bit RISC-V microprocessor, which was fabricated with *Pragmatic*'s IGZO TFT-based FlexIC process, and demonstrated to bend below a 5 mm radius of curvature.

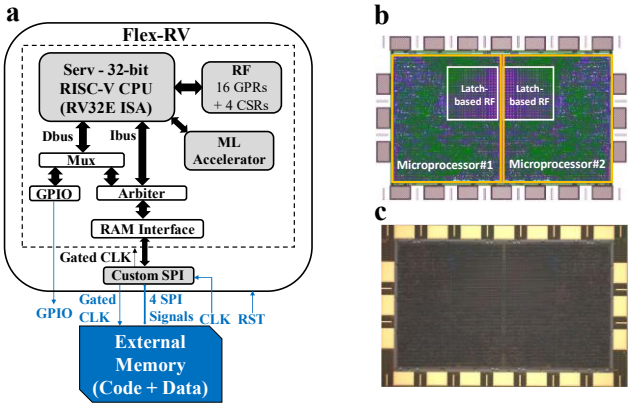


**Figure 1** a. System architecture of the Flex-RV microprocessor, b. The layout of the Flex-RV testchip containing two Flex-RV microprocessors, c. Die photo of the testchip taken under a microscope

## Flex-RV System Architecture

We use the open-source *Serv* RISC-V CPU [5] to implement the Flex-RV microprocessor. *Serv* is the smallest RISC-V CPU developed to date, and is a bit-serial CPU in which 32-bit computations are performed bit by bit rather than in parallel. This reduces the design complexity of a 32-

* Link to the video - https://www.youtube.com/watch?v=m8dJAZST_Oo
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bit RISC-V processor at the expense of performance, and its low design complexity is the main reason why *Serv* is chosen as the CPU for Flex-RV.

Flex-RV is designed to be a simple system-on-a-chip (SoC) consisting of *Serv* and additional peripherals as shown in **Figure 1a**. *Serv* is slightly modified to support the RV32E ISA to reduce the register file size to 16 registers. As the FlexIC process today does not allow us to put a sizable on-chip memory (e.g., >1kB SRAM), we opt to use an off-chip memory to access the code/data, and therefore, added a custom Serial Peripheral Interface (C-SPI) block to communicate with the external memory. The C-SPI block fetches 32-bit RISC-V instructions from the off-chip memory as well as performing 32-bit data load/store operations from/to the memory. The main reason for using the C-SPI to communicate with the off-chip memory is to reduce the number of off-chip pads to simplify the assembly process of Flex-RV onto a FlexPCB.

We also design a programmable SIMD-based ML accelerator for speeding up matrix multiplication and post-processing operations used in contemporary ML algorithms. The ML accelerator is tightly coupled to *Serv* as a custom functional unit, and four new instructions were added to the RV32E ISA so that the accelerator can be programmed.

## Fabricated Testchip Results

We implement Flex-RV using *Pragmatic*'s 0.6µm FlexIC technology that uses a unipolar logic consisting of an n-type IGZO TFT and a pull-up resistor, and fabricate them on 200mm polyimide wafers with a thickness of 30µm. The fabricated Flex-RV testchip has a 9mm×6mm die size and 20 pins, and contains two Flex-RV microprocessor instances as shown in **Figure 1b** and **c**. Each Flex-RV instance has a core area of 17.5mm$^2$, a gate count equivalent to 12,596 NAND2s, and total power consumption of 5.8 mW at 3V.

The Flex-RV testchip results show that Flex-RV assembled on a FlexPCB can run as fast as 60kHz and be bent to a radius of curvature below 5mm while still executing programs correctly (i.e., dynamic bending tests). Bendability is demonstrated using three cylinders: 3mm, 4mm and 5mm radii. We tested tensile bending mode (that is, the curvature of the chip is outward) and compressive bending mode (that is, the curvature of the chip is inward) as shown in **Figure 2a** and **b**, respectively. We perform dynamic bending tests as rolling the FlexPCB and bending the Flex-RV chip occurs while the microprocessor is running the test benchmarks. **Figure 2c** shows the "Hello World" running on the microprocessor while it is bent. You can also see the video at the link provided on the footer of the first page.

We observe two trends from the results of the dynamic bending experiments in three different bending radii: (1) Flex-RV accelerates in tensile mode but slows down in compressive mode, which is attributed to a change in the device and wire parameters. (2) As the radius of curvature decreases, its performance increases in tensile mode. This is because as the chip increases in tensile strength, the device and wire parameters change proportionally to improve the performance of Flex-RV, whereas the opposite is observed in compressive mode. The bending experiments show that Flex-RV can function correctly at a bending radius as small as 3mm, and on average, Flex-RV can operate 2.3% faster in tensile mode and 4.3% slower in compressive mode with respect to the flat position. Each microprocessor demonstrates resiliency as it can return to its highest achievable clock frequency after multiple tensile and compressive bending tests.

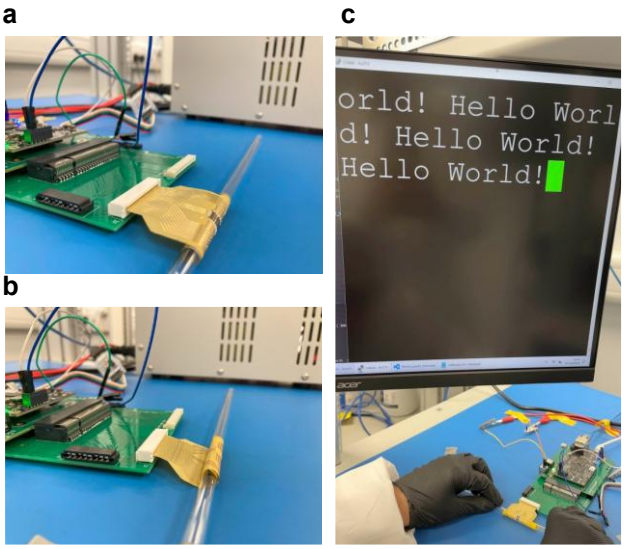


**Figure 2** a. Tensile bending mode, b. Compressive bending mode, c. A Flex-RV microprocessor is running the "Hello World" displayed on the screen while bent in tensile bending mode

## Conclusion

Flex-RV brings a new age of open-standard, non-silicon ultra low-cost 32-bit microprocessors with the potential to democratize computing access and enable new applications at Extreme Edge.

## References


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