Comprehensive Lockstep Verification for NaxRiscv SoC integrating RISCV-DV, RVLS, and Questa/UVM

Our lockstep verification framework for the **NaxRiscv** OoO superscalar core combines hybrid RTL/ISS simulation via **RVLS**, constrained-random test generation with **RISCV-DV**, and coverage collection through **Questa/UVM** to enable early detection of corner-case bugs and ensure strict ISA compliance.

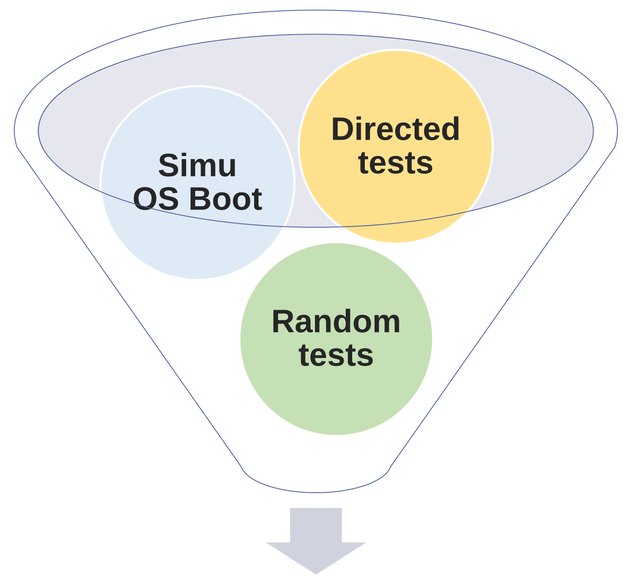
Introduction

We overcome the complexity of modern processor verification by performing lockstep co-simulation of the NaxRiscv RTL using **Verilator** and **Spike ISS**

Verification strategy

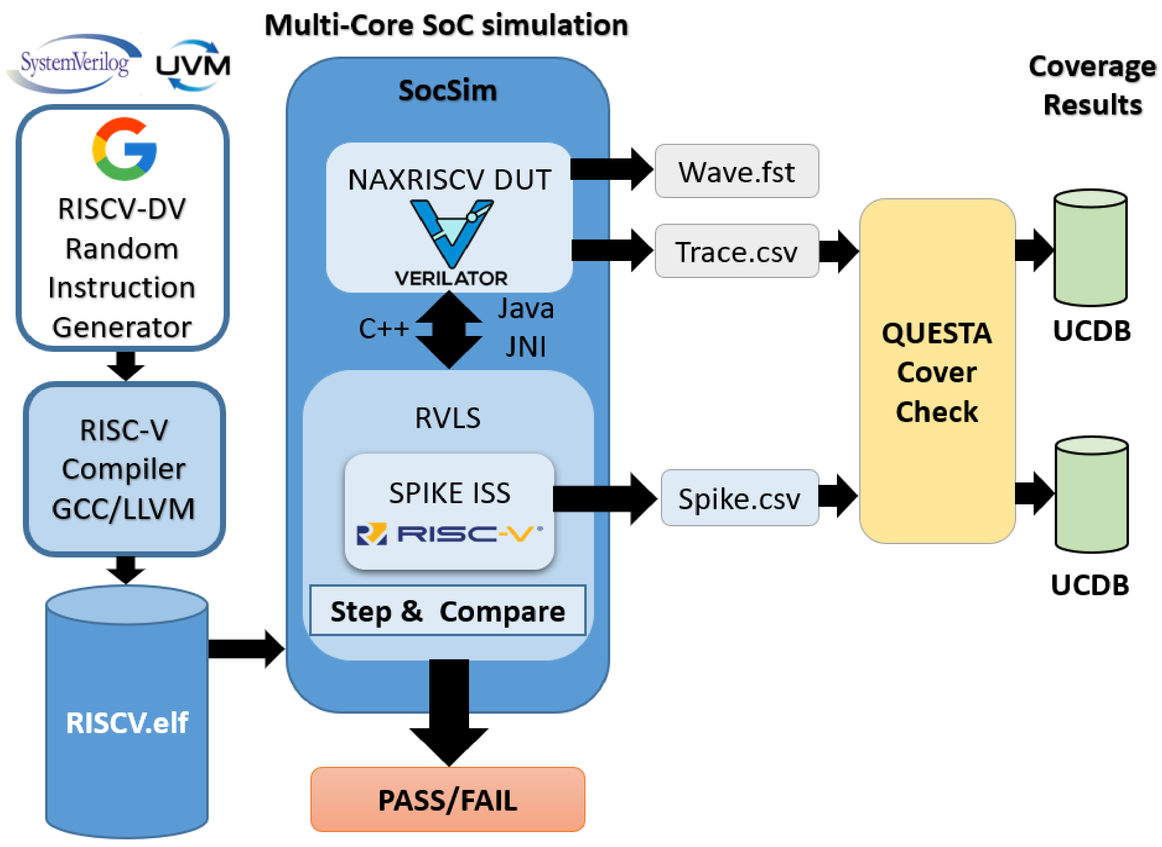
Automated Verification Pipline Powered by Jenkins CI

1. Directed Testing
   - Riscv-tests / Riscv-arch-tests (ISA compliance).
2. Real-World Benchmarks
   - CoreMark, Dhrystone, FreeRTOS/Linux boot.
3. Constrained-Random Testing
   - RISCV-DV (edge cases, interrupts, hazards).
4. Coverage Collection
   - Questa to create coverage report frome ISS trace.



Result Overview

Issue	Triggred exception
I/O memory mapping mismatch	Trap store access fault
Misaligned instructions	Load page fault
CSR configuration mismatch	Missed trap in DUT



Conclusion

- **Benefits**
  - A lockstep cycle-accurate SoC verification.
  - Fully automated Jenkins CI/CD pipline.
  - Collection of coverage reports.
  - Early detection of critical corner cases.
- **Perspectives**
  - Automation of coverage reporting merge.
  - Jenkins deploys tests on FPGA via LiTex.
  - Integration of RVFI for a formal verification.

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References

[1] https://github.com/SpinalHDL/NaxRiscv

[2] https://github.com/chipsalliance/riscv-dv