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Verification of a RISC-V system with multiple cores

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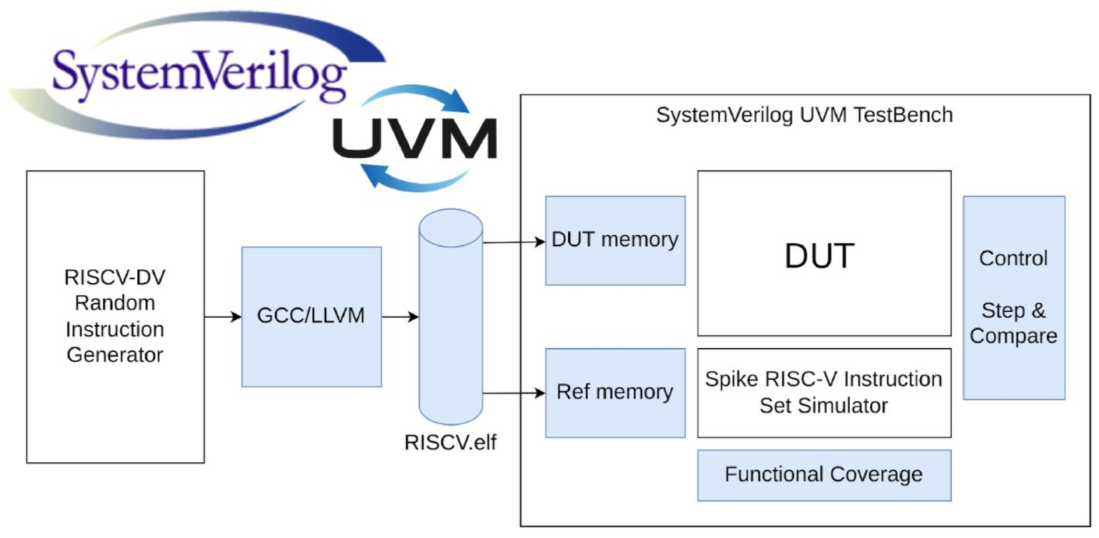
We present a verification strategy for complex RISC-V systems—especially those with out-of-order cores and multi-level cache hierarchies. Our approach leverages a reusable UVM testbench, a modified version of the Spike ISS as a reference model, and a combination of directed tests and randomly generated binaries (using riscv-dv) to achieve comprehensive coverage and bug detection.



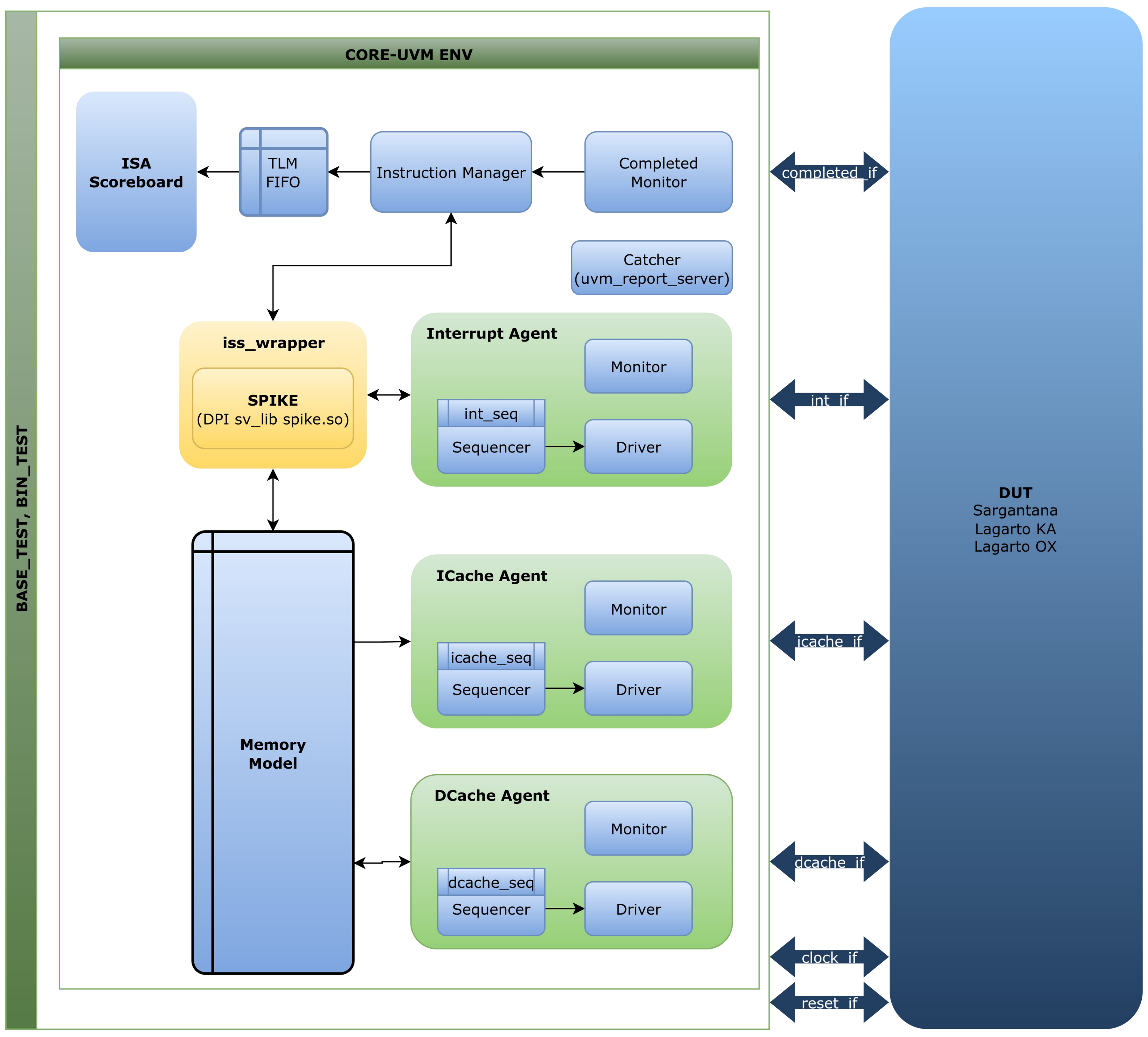
Methodology

UVM Environments

- **Core-UVM:**
  - Targets individual cores (in-order and out-of-order). We have support for three different designs: one in-order (Sargantana) and two out-of-order cores (Lagarto KA and Lagarto OX).
  - Incorporates key interfaces:
    - Complete: containing the state (PC, results, CSRs, etc.) of completed/committed instructions.
    - Interrupt: interrupt state signals, to inject interrupts to the core and detect when it traps.
    - Data and Instruction cache signals.
  - Uses a scoreboard to compare execution outcomes with the reference model.
- **CPU-Subsystem UVM:**
  - Verifies a system-level design integrating multiple cores (operated individually) and three cache levels.
  - Includes Core-UVM in passive mode
  - Includes additional components:
    - AXI - Slave Memories to emulate main memory, SRAM and bootrom. Modelled using the AXI-mem component from the Pulp project.
    - AXI - Master VIP to support verification of DMA bridge and be able to exchange and access different design blocks of RTL through DMA.
    - JTAG - VIP to verify JTAG protocol and RISCV debug module.
    - PLIC / CLINT UVM agents to generate external, timer and software interrupts at the subsystem level and verify its handling by the RTL.
    - UART model. An AXI crossbar from the Pulp project is used to connect both an SRAM and the UART to the peripheral bus.

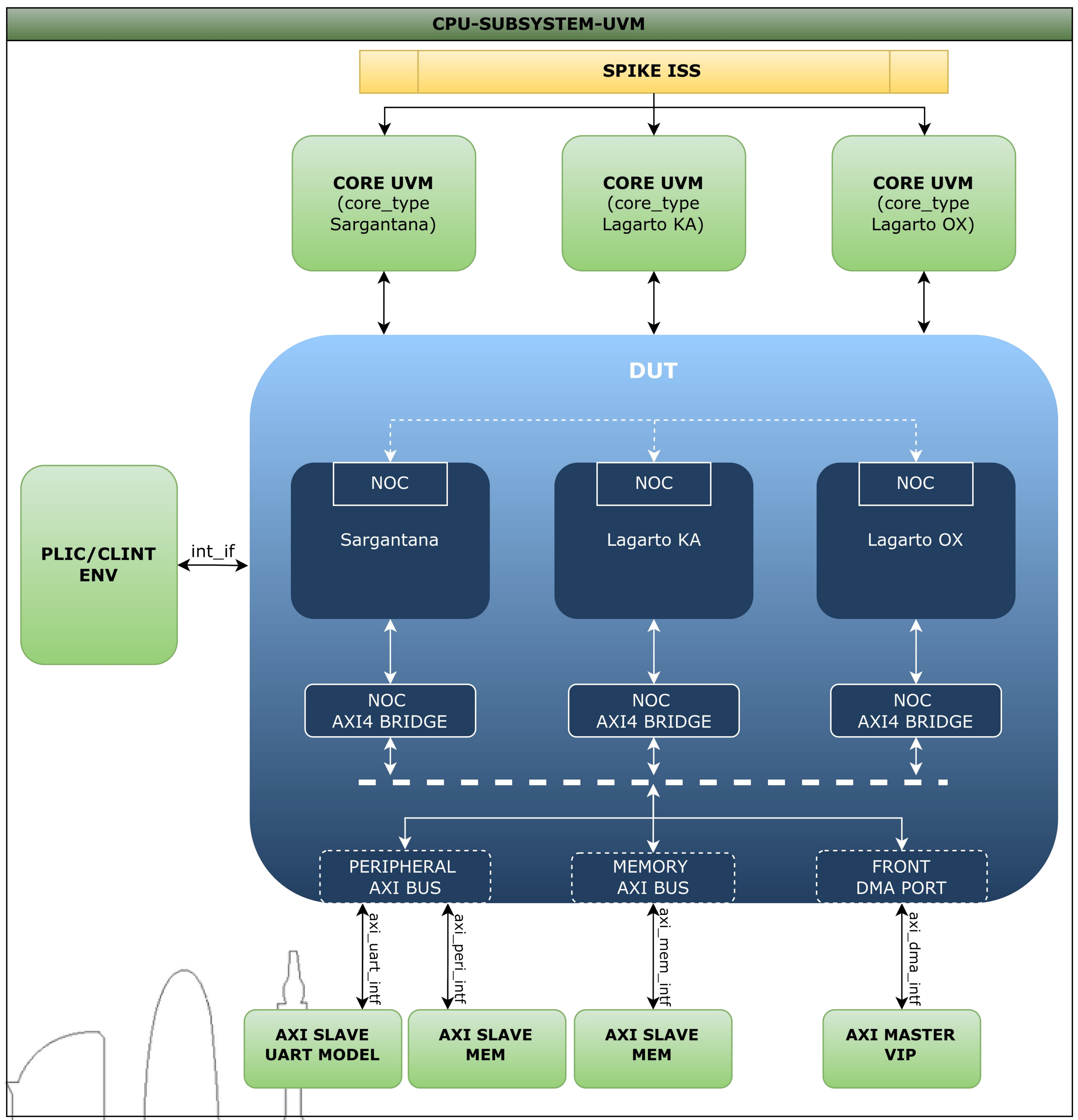
Reference Model

- **Modified Spike Instruction Set Simulator:**
  - Enhanced with SystemVerilog DPI calls to interact with UVM, for step-by-step cosimulation.
  - Main DPI functions are:
    - To execute last committed instruction and return the simulator state.
    - To change external/timer/software interrupt behavior (in order to mimic the core's ack of the interrupts).
    - To perform a TLB walk without triggering exceptions (to model VIPT caches in core-uvm).
    - To force RTL results into Spike (due to a few known bugs of floating point rounding errors, values of hpm counters, etc.)
  - Supports configuration flags (e.g., core_type) to emulate various design behaviors (e.g., reset values of some CSRs, supported vector instructions, etc.).



Testing Strategy

- **Directed Tests:**
  - RISCV-isa-tests.
  - RISCV-arch-tests (formerly compliance tests).
  - Internally developed ISA tests.
  - UVM directed tests for verifying the JTAG and DMA interfaces
- **Randomized Tests:**
  - Generated using a modified version of RISCV-DV to uncover corner cases and bugs.
  - Modifications include:
    - Full support of RVV 1.0 vector extension.
    - Vector memory instructions generation with changing values of SEW and vector length.
    - Finer control of the randomization of key registers (ra, sp, tp, etc.).
    - Extension and customization of the trap delegation system.
- Incorporation of constrained random testing and assertion checks.



Conclusions

- **Key Contributions:**
    - A reusable UVM testbench adaptable for both core and system-level verification.
    - Enhancements to the Spike ISS for improved simulation fidelity.
    - A robust combination of directed and randomized testing methodologies that substantially improve coverage and bug detection.
- **Future Work:**
    - Extending the verification environment for simultaneous multi-core operation.
    - Contributing tool enhancements back to the community for broader use.

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