HW-extended containers on FPGA-based RISC-V SoC

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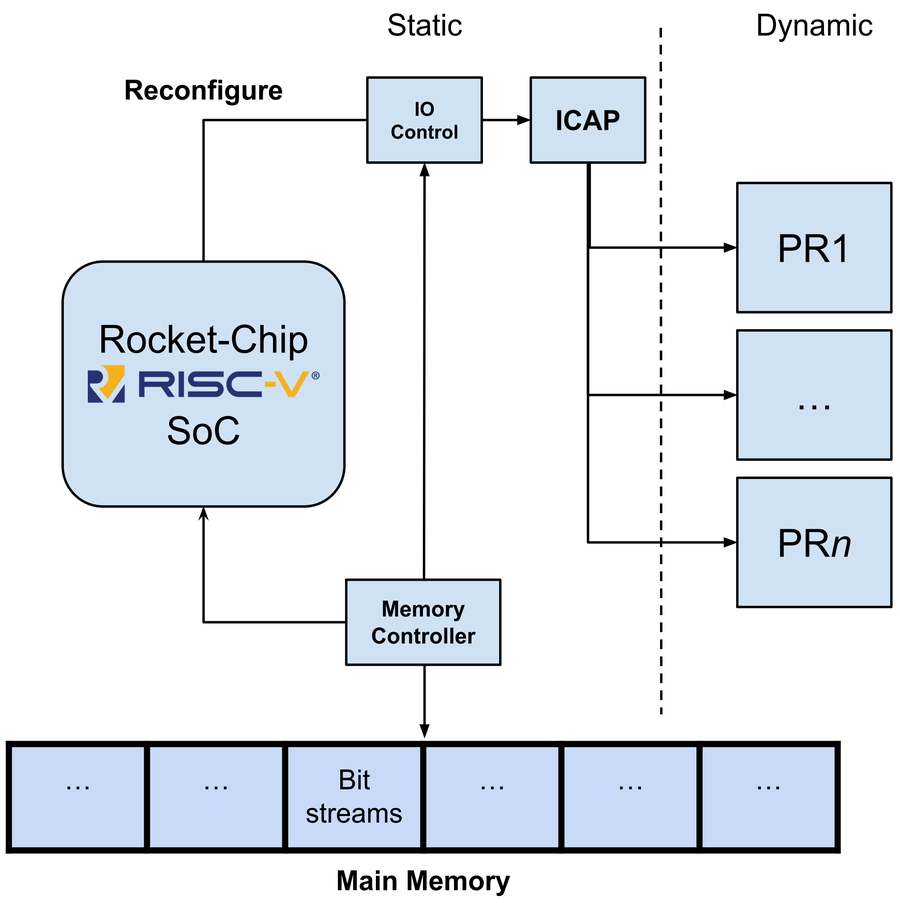
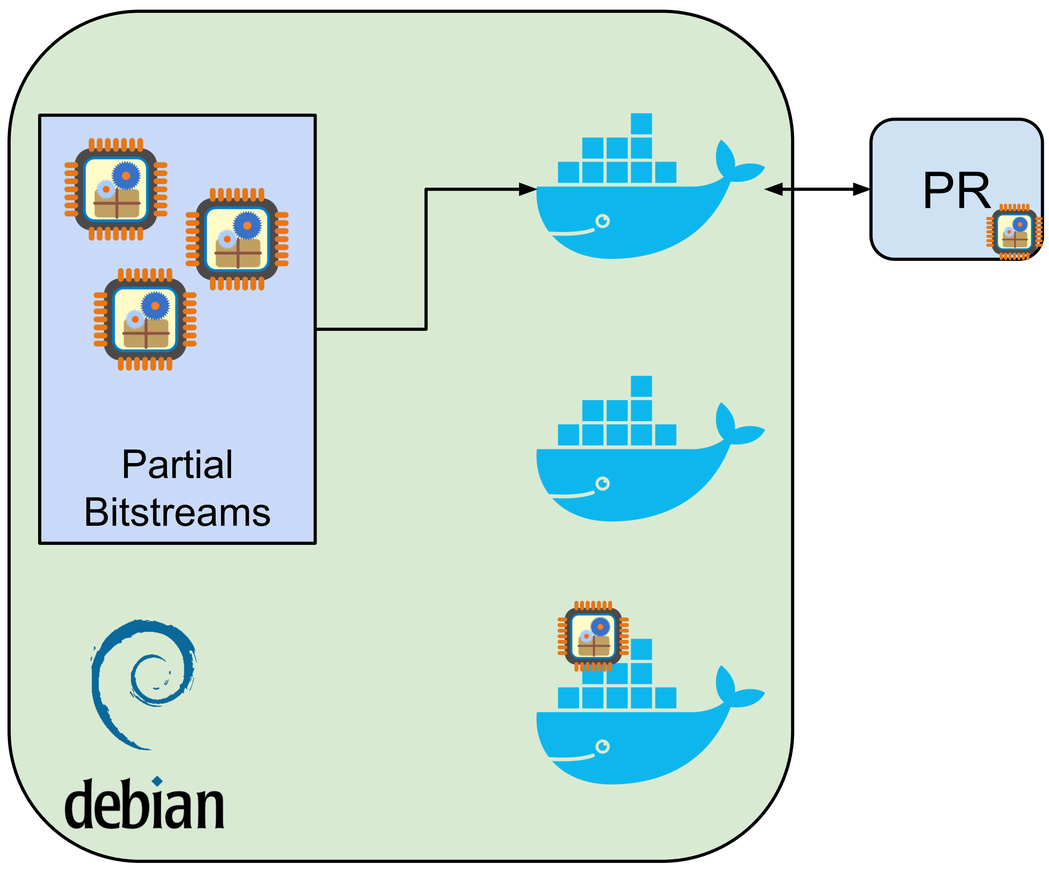


Hardware overview

- Static part
  - Configurable (core count, cache) Rocket-Chip SoC
  - High-Bandwidth ICAP
  - Per-region DFX decoupler
- Dynamic Part
  - Programmable regions
  - AXI4-lite communication protocol
- Prototype on AMD Xilinx VC707 FPGA

Software overview

- Debian based Linux
  - All kernel options and modules for Docker functionality
  - Kernel version 6.3.4
- Docker
  - Use a set of available partial bitstreams
  - Ship with customized bitstreams
  - RISC-V community-maintained distribution
- Utilities
  - Tools for checking reconfigurable region availability
  - Functions for programming partial bitstreams
  - Bitstream driver template
  - Custom scheduling interface



Future Work

- Evaluation
  - Reconfiguration performance
  - Runtime performance
    - Regular benchmark vs accelerating the core benchmark routine
  - Region scheduling evaluation
- Wider set of partial bitstreams
  - Security functions
  - AI accelerators
  - Cryptographic accelerators

Applications

- Post-design Hardware testbed
  - Check the suitability of SoC – accelerator configuration
- OTA hardware update capabilities
  - Adapt to novel AI acceleration requirements
  - Update faulty or outdated accelerators
    - e.g. cryptographic modules
  - Update hardware where physical access is limited
    - e.g. Space
- Repurposing
  - The SoC can be repurposed by configuring new bitstreams on demand

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