Codasip X730: the world's first commercially available CHERI-RISC-V application core

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→ The memory safety problem

Memory safety vulnerabilities are costly. For example, losses due to the well-known OpenSSL heartbleed bug are estimated to exceed $500 million. So there is increasing interest, even from the White House and UK government, to mitigate these vulnerabilities.

Even the best programmers can introduce memory-related software bugs! Thus, memory safety continues to cause widespread and costly cyber security problems.

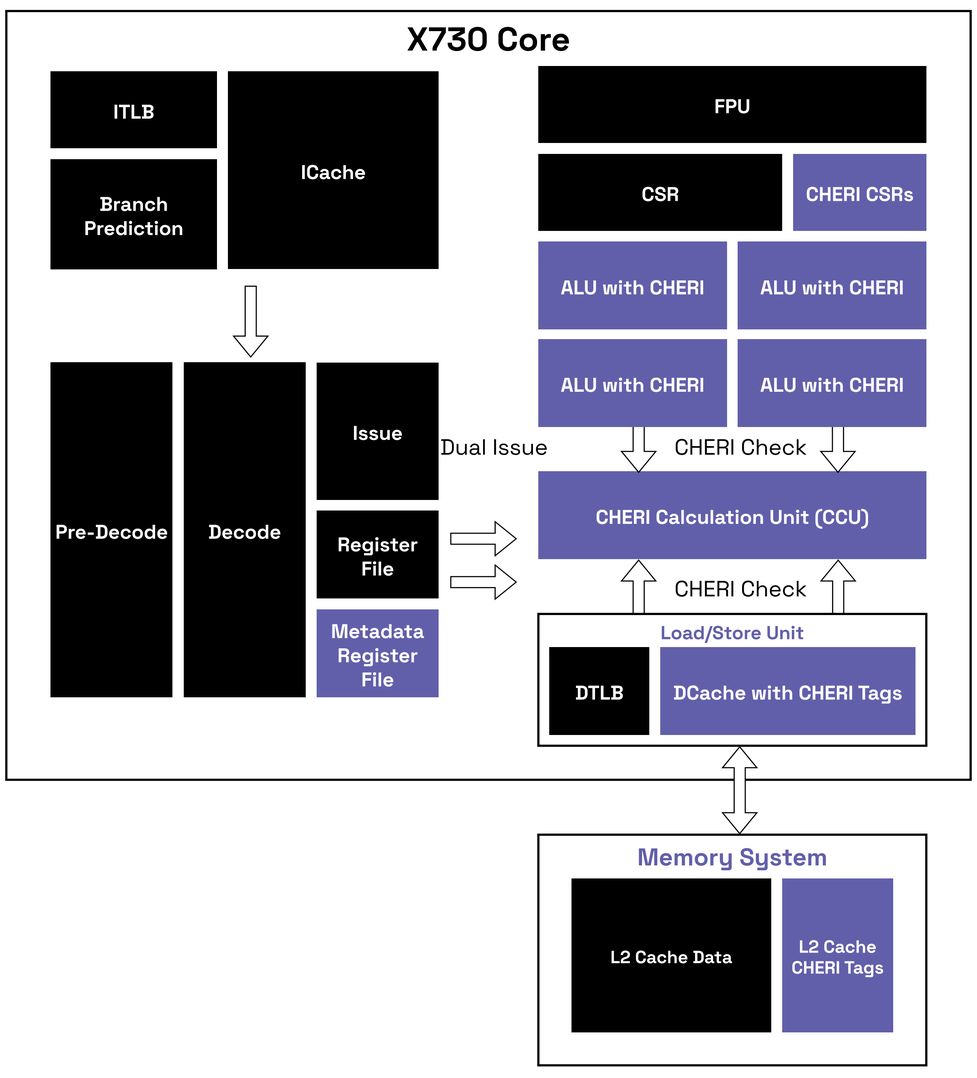
→ CHERI effectively prevents memory safety issues

The Capability Hardware Enhanced RISC Instructions (CHERI) provide a solution to memory access vulnerabilities, compartmentalization and control flow integrity without having to re-write all software.

Codasip is standardizing a CHERI extension for RISC-V in collaboration with the University of Cambridge and Google. The first commercial implementation of the new CHERI-RISC-V extension is the X730 application core.

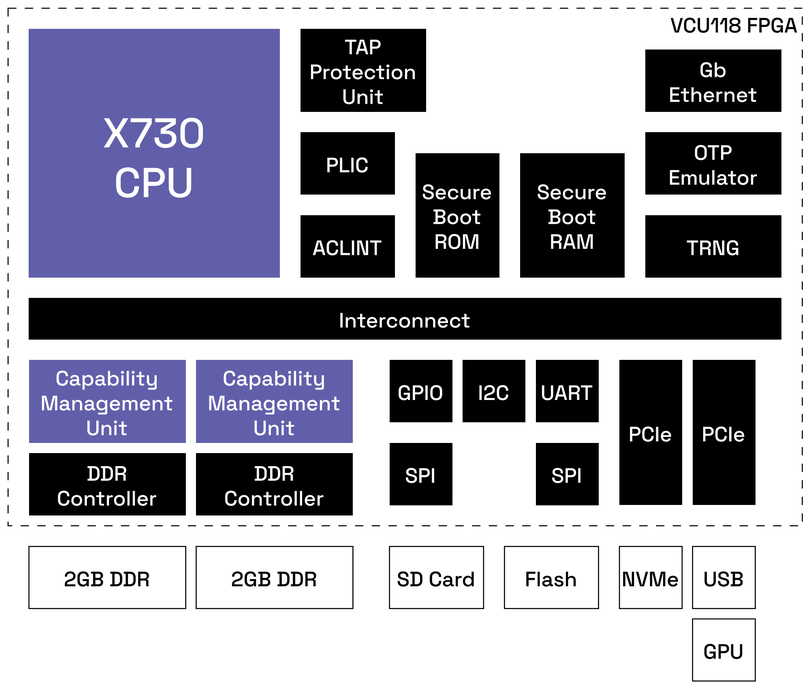
→ Codasip X730 implements CHERI-RISC-V

- X730 is written using Codasip's CodAL processor description language to maximize customization.
- The baseline 64-bit, dual-issue microarchitecture has been extended to efficiently handle capabilities and implement CHERI's new instructions and functions.
- The register file, and some CSRs, are extended to 129 bits to accommodate capabilities.
- The memory system is extended to atomically handle capability tags while still using standard interfaces.
- The performance is comparable to the the baseline microarchitecture at the cost of about 4% more area.



→ Codasip X730 evaluation platform

We are putting together a comprehensive hardware platform with a full software development kit. The platform will be suitable for evaluating and demonstrating the capabilities of CHERI technology, developing and running CHERI software, and integrating CHERI hardware into wider test systems.



Running Linux on X730 with CHERI

→ Coming soon: Codasip V730

V730 is based on a 32-bit, dual issue, in order microarchitecture. It has the same pipeline as X730 with 4 ALUs, but without the L2 cache.