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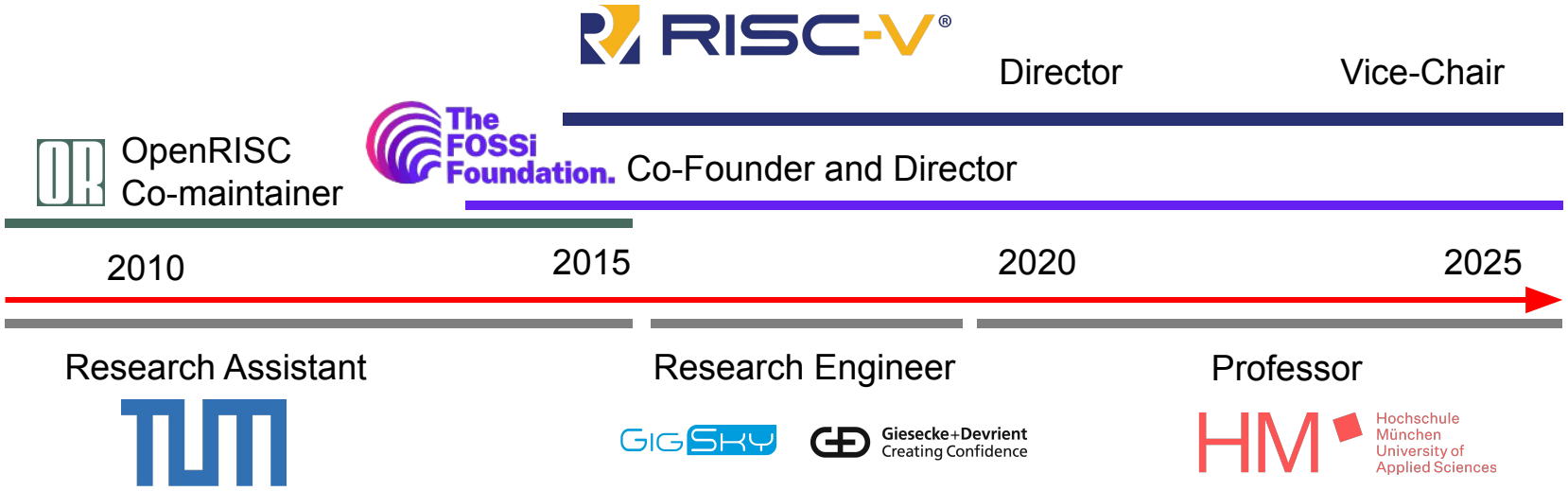
Open Source Chip Design in the European Semiconductor Strategy

Stefan Wallentowitz

RISC-V Summit Europe

May 15, 2025

About me


RISC-V
Director
Vice-Chair
OpenRISC
Co-maintainer
The FOSSi Foundation.
Co-Founder and Director
2010
2015
2020
2025
Research Assistant
Research Engineer
Professor
GigSky
Giesecke+Devrient
Creating Confidence
HM
Hochschule München
University of Applied Sciences

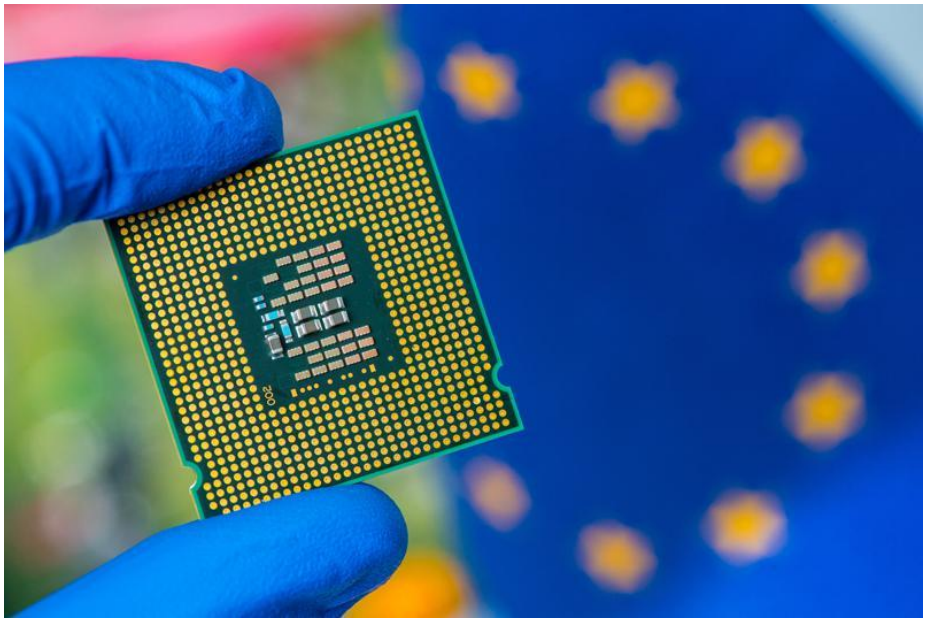
Chip Design Ambitions in Europe and Germany

Ignited by *global supply chain* and *geopolitical challenges*

Chips are a *strategic asset*, key ingredient of the *digital transformation*

Investments and strategic policies *across the globe*

European Chips Act and intensified national funding



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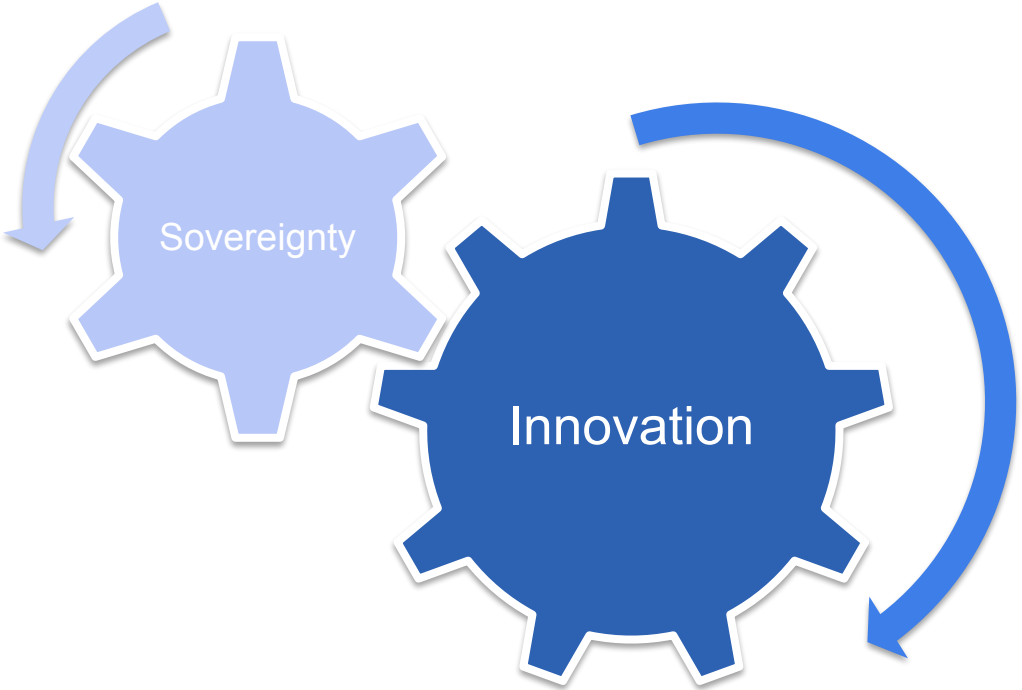
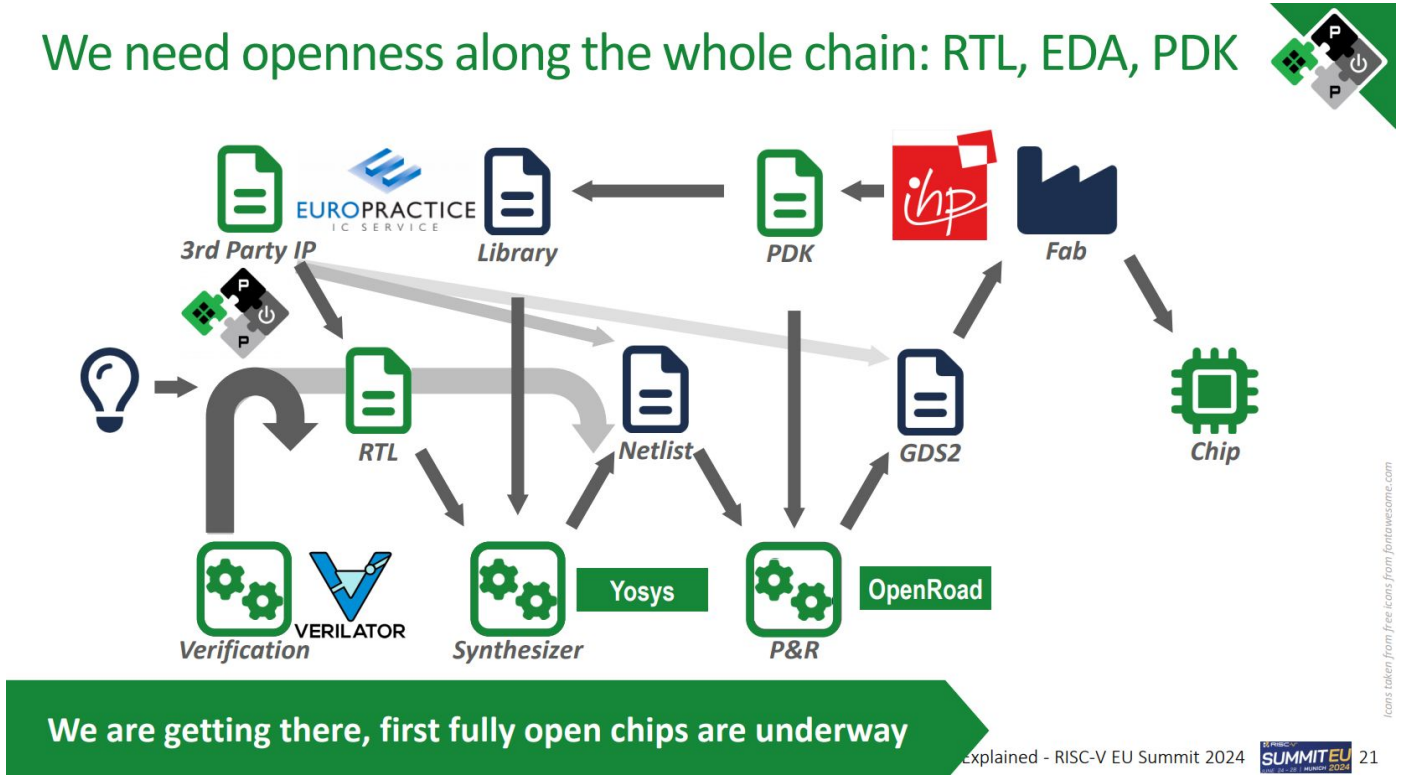
Drivers for sustainable chip ecosystem



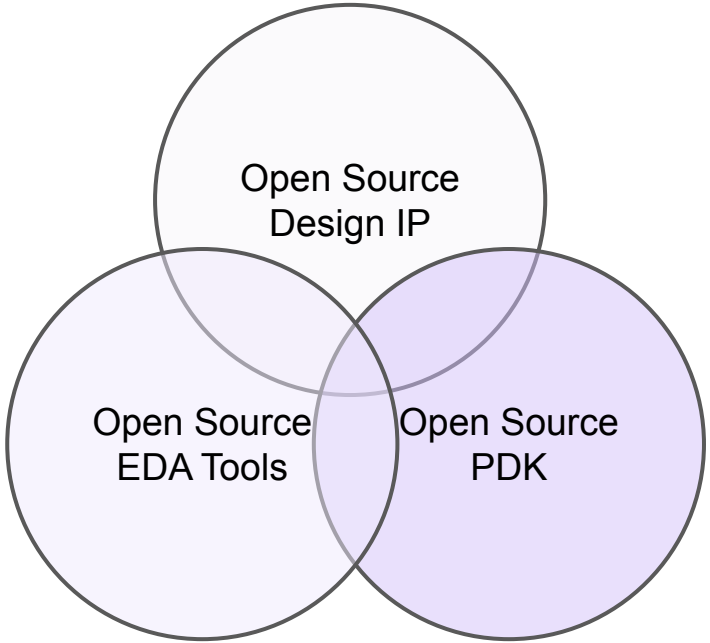
Open Standards and Open Source

- RISC-V is an open standard, backed by open-source implementations since its inception
- Reference implementations and easy-to-extend open-source designs make it easy to learn and innovate
- Open-source designs had especially in Europe a huge impact on the success of RISC-V

Towards Open-Source Chips



Principle: Each part can be used separately

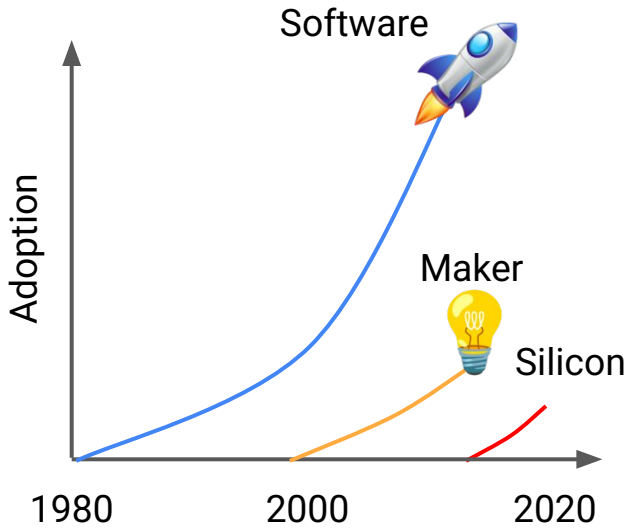


Full Open-Source Chip

- **First end-to-end open-source**
- **Application-class SoC (Linux)**
- **Based on open-source**
  - Design IP: CVA6 RISC-V
  - EDA Tools: Yosys, OpenRoad, etc.
  - Open source PDK: IHP 130nm

Comparison to Open-Source Software

- **Open Source Software**
  - “Release early, release often”
  - Limited costs of updates, patents not really an issue
- **Open Source PCBs, “Maker”**
  - Costly revisions, hard to fix
  - Complexity can be handled, manufacturing is key issue
- **Open Source Silicon**
  - Extremely costly revisions, no fixes
  - Manufacturing and tools complex



Why do we need open-source chip design in Europe?

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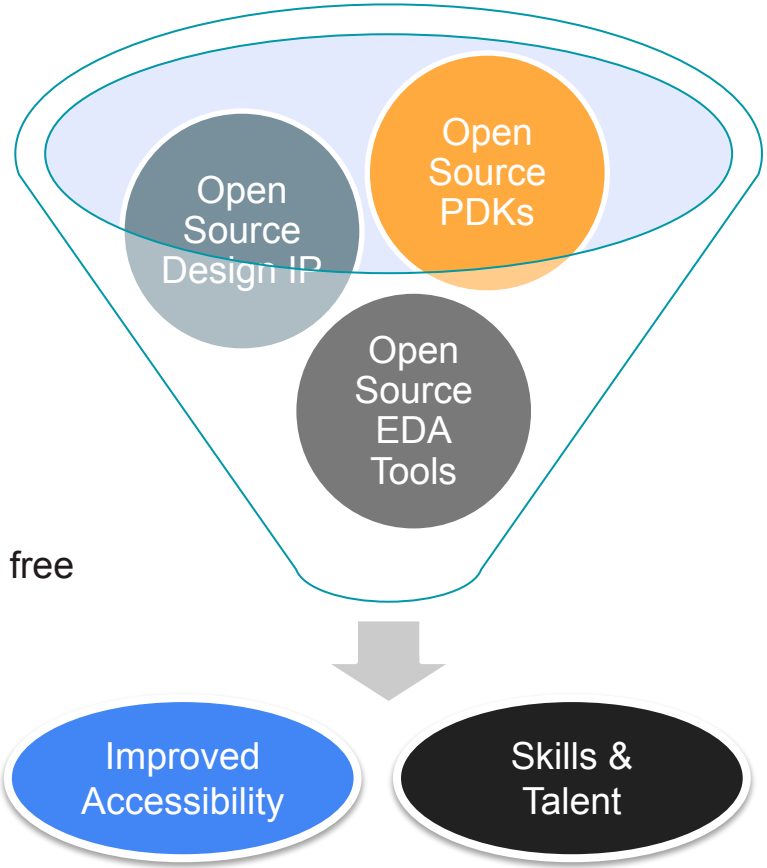
Direct Impact

Enable SMEs and Newcomers

- Remove burdens, gain experience
- Some technologies can already be served

Nurture Talent Pool

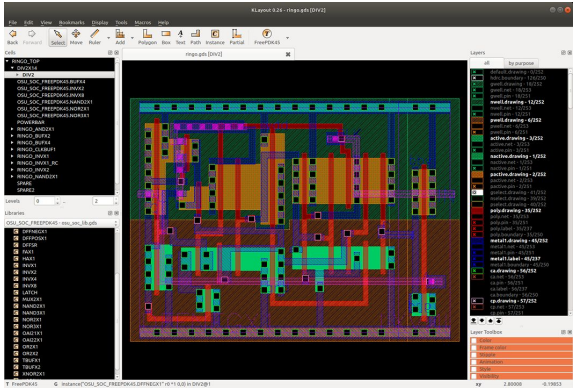
- Attract new talent, better accessibility, no NDA, free
- Gain insights into the actual tools



Open-Source Design IP

- **Strong history in Europe: OpenRISC, LEON, etc.**
- **Significant boost with RISC-V**
  - Driven from academia & industry R&D
  - Funding for commercialization via Chips JU
- **Non-core IP still lagging behind**
- **Sustainability and adoption challenges**

Open Source EDA



Highly specific software tools with niche user base

Open Source EDA for layout available since 80s

Selected highlights:

- Verilator enables industry to run continuous integration everywhere
- Python-based Verification increases productivity
- OpenROAD is a full design flow with goal of chip design in 24h

Open Letter

> 500 signatories

Main arguments:

- Open-source EDA tools lower the barrier of entry significantly for students and researchers
- Open-source EDA tools allow researchers and designers to collaborate easily
- Open-source EDA tools are, for themselves, interesting for innovations, research, and development

https://open-source-eda-letter.eu/

Importance of Open-Source EDA Tools for Academia

Open Letter on European Strategic and Funding Directions

To Whom It May Concern

March 8, 2024

The recent semiconductor shortage and shifts in global political relations have changed the European roadmap on semiconductors and chip design significantly. A mix of incentives for new fabrication facilities for advanced technologies and the ambitious goals to (re)-build leading-edge chip design capabilities in Europe are key cornerstones of the European Chips Act. Under this impulse, various funding actions have been successfully launched, for instance in the area of the creation of IP based on the RISC-V instruction set.

Roadmap and Recommendations

Tasked by Chips JU

Goal: Support Funding Decisions

Intensive community effort

Released in November 2024

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Recommendation: Three Actions

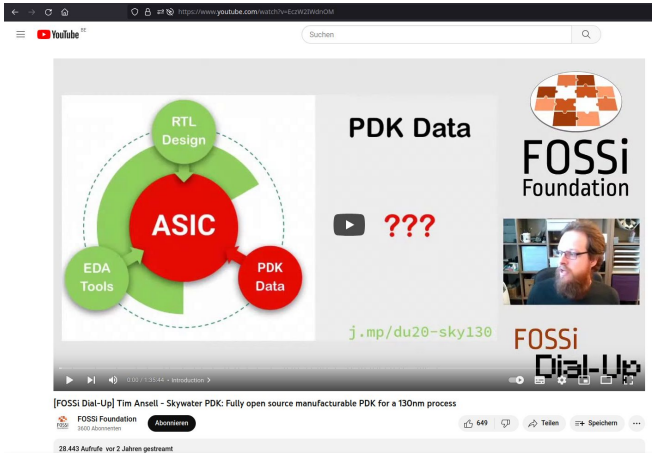
	Impact	
	Key Industries & SME	Talents
Action 1: Open-Source Analogue and Mixed-Signal Designs for Europe	++	+
Action 2: Productivity, Interoperability and Verification for more European Chips	+	++
Action 3: System-on-Chip Innovation from Europe with Open-Source Digital Chip Design	+	+

HORIZON-JU-Chips-2025-IA-EDA

- **Chips for Europe Initiative Call**
- **Indicative Budget: 20 Million Euro (+20 Million national co-funding)**
- **Three streams (each one consortium, strongly tied)**
  - Digital SoC design
  - Analogue and mixed-signal design
  - Productivity, interoperability, and verification
- **Project Outline deadline ended on April 29**

Open Source PDK

- **Process Design Kit (PDK) contains actual physical design elements**
- **Push for manufacturable PDKs by**
  - Google with Skywater PDK (130nm) and GlobalFoundries (180nm)
  - IHP 130nm BiCMOS in Germany



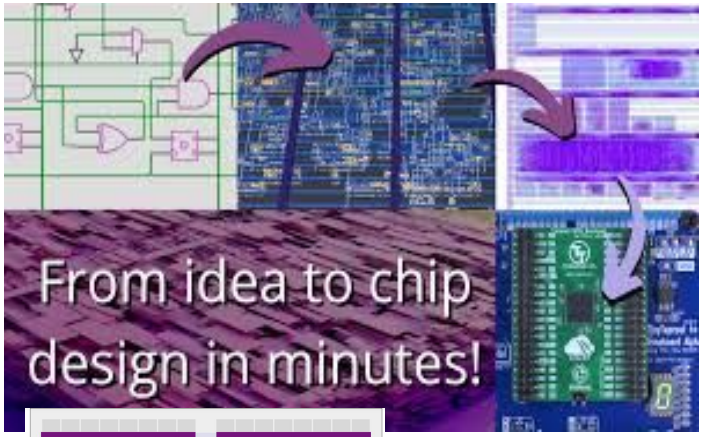
Fabrication Access

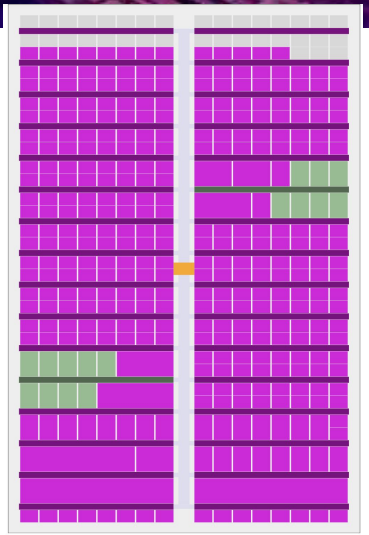
PDK is great, building a chip is better!

Affordable, regular production runs needed

Tiny Tapeout as low barrier entrance:
Own Chip for $300

Goal: one student one chip





Open Letter 2

- Sustainable open source PDK access
- One-student-one-chip for European students

https://open-source-chips.eu/

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Open Source Chips for Europe

Open Letter on the Urgency of Access to Open Source Chip Manufacturing

To Whom It May Concern

March 31, 2025

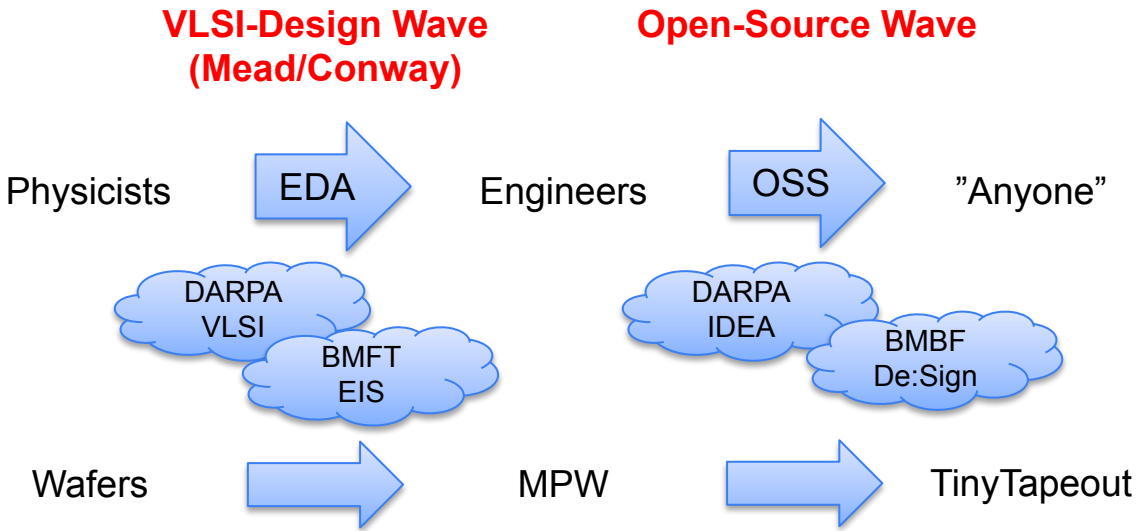
The European Chips Act has set ambitious goals and its implementation is a significant pan-european effort. From an academic perspective, last year we published an open letter emphasizing the critical importance of open-source EDA for academia in Europe. We were excited and grateful to see that this initiative triggered the definition of a European roadmap in this area, and a matching Chips JU call for project funding. We believe that the projects funded by this call will have a significant impact. Moreover, we already see rising interest from many EU stakeholders, with increasing investments into open-source chip design, especially in open source IP development (e.g. RISC-V cores), and open source EDA tools.

One additional critical barrier remains toward the end-goal of building real open-source chips, especially for prototyping and education: namely, **streamlining the access to open source chip production facilities (foundries) is essential**. Programs like ChipIgnite, Tiny Tapeout and IHP's open source program have become "guiding stars" that demonstrate that everyone with a computer can build chips. We believe that having low-cost, regular and easy access to chip production is critical to create excitement and build up expertise, widening the pool of chip designers with tape-out experience: a true **silicon democratization** and a further **de-mystification of chip design**,.

Currently, academia and companies can get affordable access to chip manufacturing via EUROPRACTICE-IC, which has been instrumental in supporting IC design in Europe and has so far enabled hundreds of designs to be manufactured. Each silicon manufacturer (foundry) provides a set of rules and configurations that help designers ensure that their ICs can be reliably

Summary

Open source can be the next *demystification* of Chip Design



Join the community!

free to attend!

ORConf 2025

September 12 - 14, 2025
Valencia, Spain

https://orconf.org

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Thank you!

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