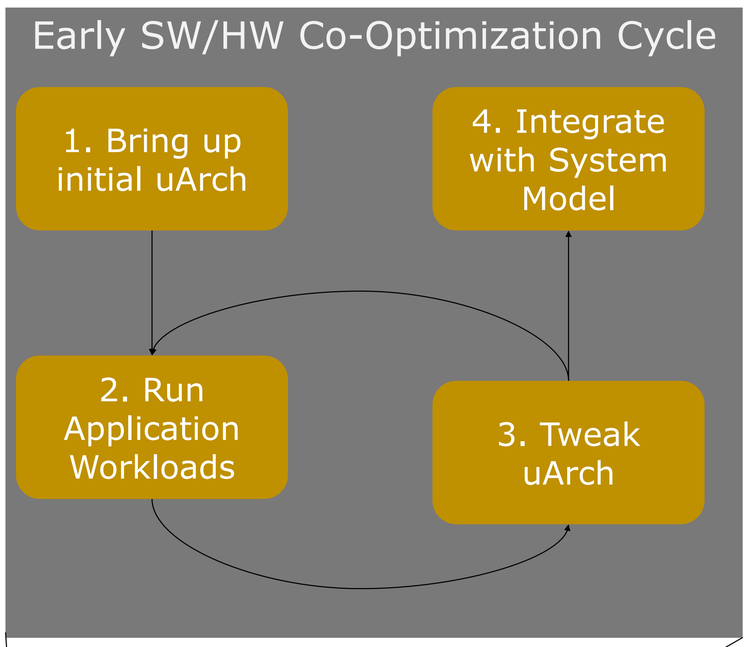
Enabling Software and Hardware Co-Optimization

Analyze real-world workloads with deep insights into micro-architectural function and efficiency with high-fidelity processor modeling technology



Optimize at the System-Level

- Standard TLM interfaces enable a system-level platform for software development
- Works with Virtual Platform Tools like ImperasFPM and Virtualizer

Atlas Explorer enables early customer access

- Integrated solution for fast customer on-boarding and broad-base utilization
- Comprehensive micro-Architectural reports for I8500, M8500, and all future MIPS Processors

Workload Exploration → Iterate and improve HW for workload → System Software Integration and CI - CD → System-Level Correlation → System Software Improvements → Support Software throughout the Product Life Cycle

Architectural Exploration | SoC Development | Support and Maintenance

WIP

Optimization Tools
- Function, memory, pipeline explorers

Add system arch diagram (see Synopsys simulation overview)

Software Development
- Build, debug, test software programs and libraries
- Simulation Trace Format

Add details of STF record capture

Simulation Technologies
- Instruction set simulator of RISC-V processor
- Performance model of processor microarchitecture

Add details of ISS and Performance model

