Building the RISC-V Education Ecosystem: A Systematic Educational Contents Design, Remote Laboratories, and Community-Driven Learning

Yunxiang Luo, Fuyuan Zhang, Tianwei Jiang, Zhi Li, Hang Zheng, Xirui Hao

Institute of Software, Chinese Academy of Sciences (ISCAS)

Abstract

The widespread adoption of RISC-V technology is facing with significant challenges, particularly the deficient talent cultivation system, which severely restricts its ecosystem growth. This paper investigates core issues in RISC-V education within China, including a shortage of skilled professionals, fragmented curriculum resources leading to low learning efficiency, scarcity of high-quality educational content, insufficient experimental equipment hindering programming capabilities growth, and a dispersed technical community with weak collaboration. To address these challenges, a systematic educational solution is proposed, encompassing tree dimensions: curriculum development, experiment environment support, and community engagement. In curriculum design, collaboration occurs with our laboratory, community developers, and university teachers to construct a multi-tiered course system spanning from foundational theories to cutting-edge technologies. A quality assurance mechanism is established through weekly technical seminars to form a course quality grading methodology ensuring continuous refinement of educational content. In order to address the challenge posed by hardware resource limitations, a strategy of integrating laboratory facilities across multiple regions in China has been adopted, with the aim of establishing a remote experimental environment that supports diverse RISC-V boards. This approach has the effect of significantly lowering barriers to RISC-V experimental environment access. Furthermore, an active community is cultivated, reaching over 30,000 participants through Bilibili and WeChat communities, regular offline technical workshops, and RISC-V programming competitions, fostering learner engagement and technical identity. The results demonstrate that this solution has produced over 1,000 original instructional videos, which have accumulated more than 1.3 million views. This systematic approach not only addresses critical educational gaps but also provides a scalable model for nurturing talent in emerging technologies, thereby accelerating the integration of RISC-V into innovation landscape.

Introduction

RISC-V is an open-source and royalty-free instruction set architecture.[1] It offers flexibility, scalability and cost-effectiveness, attracting academia, industry and open source communities as an alternative to ARM and x86. However, its software ecosystem is still nascent, creating challenges and opportunities for educators and developers to drive adoption. At present, the number of individuals proficient in RISC-V development is relatively small, and the availability of comprehensive educational resources is limited.On one hand, technical documentation and course materials are fragmented, lacking coherent case studies that span from instruction sets to operating system porting. On the other hand, building hardware experimentation platforms is even more challenging, as the global availability of RISC-V development boards is significantly lower than mainstream architectures, coupled with higher costs, making it difficult for most students in non-tier-1 cities to access hands-on opportunities. Additionally, support from open-source communities remains decentralized, with technical issue resolution cycles markedly longer than those in mature ecosystems, further exacerbating the difficulties in talent cultivation.

Methodologies

To address the challenges identified in RISC-V education and ecosystem development, we propose a three-pronged approach encompassing curriculum development, remote laboratory infrastructure, and community-driven engagement.

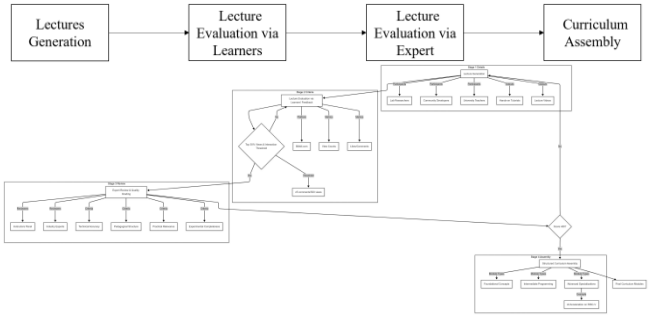

Figure 1. The curriculum design process.

The curriculum design process follows a systematic four-stage workflow, referencing Figure 1, ensuring quality control and adaptability to evolving technological trends. First of all is the lecture generation, weekly seminars are

conducted with laboratory researchers, community developers, and university teachers to identify high-impact projects and translate them into lectures. These sessions produce hands-on tutorials, and lecture videos. The second step is lecture evaluation via learners' feedback, all lectures are published on Bilibili.com, where learner engagement metrics (e.g., view counts, likes, comments) are monitored. Videos ranking in the top 30% of views and meeting predefined interaction thresholds (e.g., ≥5 comments per 500 views) proceed to formal review. The third step is expert review and lecture quality grading, a panel of instructors and industry experts evaluates shortlisted materials using a scoring rubric, referencing Table 1. Criteria include technical accuracy, pedagogical structure, practical relevance, and experimental completeness. Courses scoring ≥80 are certified for integration into the formal curriculum. The last step is structured curriculum assembly, the approved courses are organized into tiered modules, spanning foundational concepts, intermediate programming topics, and advanced specializations (e.g., AI acceleration on RISC-V).

Table 1: Course Evaluation Rubric.

Criteria	Description
Technical Accuracy	Alignment with RISC-V specifications
Pedagogical Structure	Logical progression and clarity of content
Practical Relevance	Real-world application and hands-on utility
Experimental Completeness	Inclusion of lab exercises and assessments

To mitigate RISC-V laboratory infrastructure accessibility barriers, a distributed remote lab environment was established across Beijing, Nanjing, and Shanghai, referencing Figure 2, Key components include multi-region RISC-V boards integration, access architecture, and Operating System support. The physical RISC-V development boards (e.g., HiFive Unmatched, Licheepi4A) are pooled from our labs and community contributors, enabling shared access via remote protocols. Users connect through SSH and VNC protocols, facilitated by a jump server for secure authentication. Smart power outlets enable remote power cycling, while SD Mux devices automate firmware flashing (e.g., using SDWireC for unattended SD card programming). A compatibility RISC-V Operating System Matrix, offering 56 types of RISC-V boards and 41 types of operating systems, ensures seamless integration of diverse RISC-V boards with Linux distributions (e.g., Fedora RISC-V, Debian) and real-time operating systems (e.g., FreeRTOS).

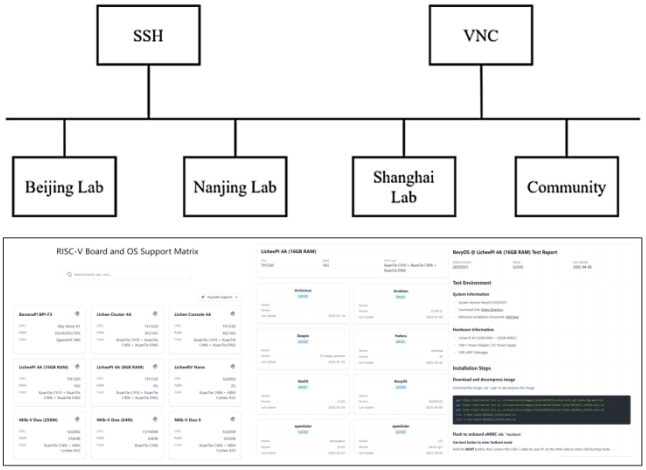

Figure 2. The curriculum design process

To foster collaboration and engagement, a hybrid online-offline community was cultivated. The community has Bilibili and WeChat host over 30,000 participants, offering tutorials, Q&A forums, and live coding sessions. Offline workshops and annual RISC-V programming competitions provide training and job opportunities.

Results

The success of this initiative is evident from the engagement metrics on platforms such as Bilibili.com, referencing Table 2. The primary channel, comprising 748 videos, has garnered 1.29 million views, 37,000 likes, and 24,000 followers. Notable series include "RISC-V Software Porting and Optimization Championships," "KSCO's Hands-on RISC-V High-Performance Simulator," and "From Scratch: Writing a RISC-V Compiler." A second channel, comprising 111 videos, has garnered 41,000 views, 1,876 likes, and 462 followers, featuring series such as "RISC-V Computing Floating Bridge" and "WiringX for Milk-V Duo."

Table2. Data from our two Bilibili.com channels

Metric	Primary Channel	Secondary Channel	Total
Number of Videos	748	111	859
Total Views	1.294 million	41,000	1,294,410
Total Likes	37,000	1,876	38,876
Total Followers	24,000	462	24,462

References

[1] E. Cui, T. Li and Q. Wei, "RISC-V Instruction Set Architecture Extensions: A Survey," in IEEE Access, vol. 11, pp. 24696-24711, 2023, doi: 10.1109/ACCESS.2023.3246491.