

Building the RISC-V Education Ecosystem

—— A Systematic Educational Contents Design, Remote Laboratories, and Community-Driven Learning

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Motivation

While RISC-V has emerged as a promising open-source ISA, its educational ecosystem remains underdeveloped. Most course materials are fragmented, lacking clear progression from fundamentals to real-world applications. Hands-on experimentation is often out of reach for students due to the high cost and limited availability of development boards, especially outside major metropolitan regions. Moreover, the absence of an active, centralized learning community slows down knowledge exchange and learner retention.

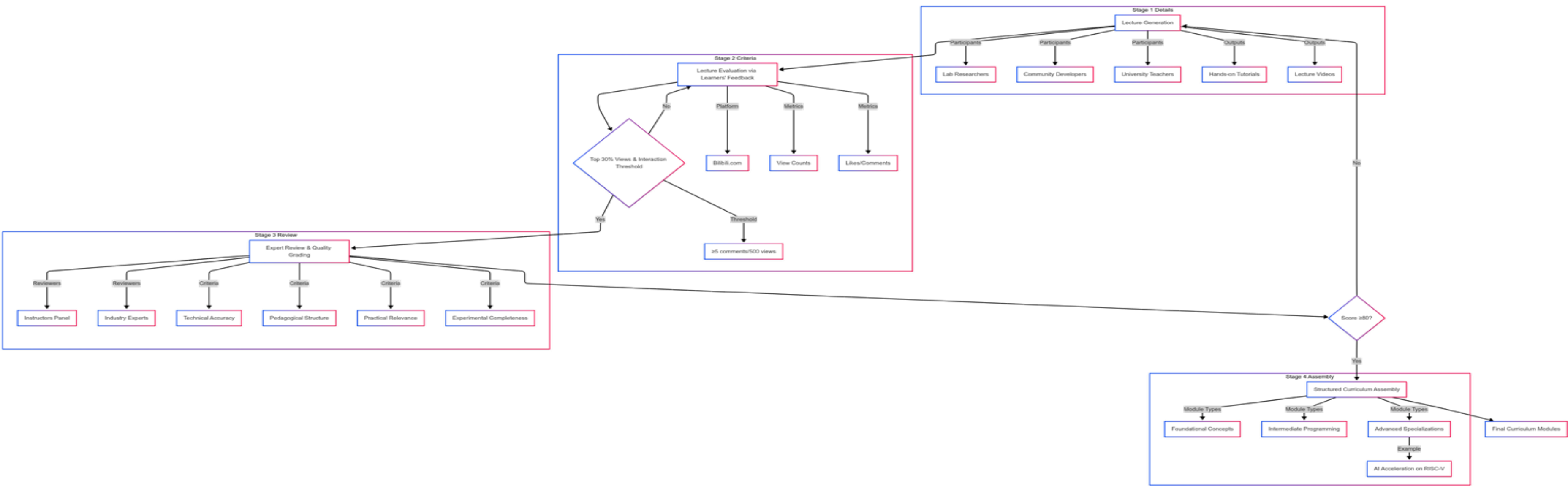
Curriculum Framework

To address the challenges identified in RISC-V education and ecosystem development, we propose a three-pronged approach encompassing curriculum development, remote laboratory infrastructure, and community-driven engagement.



The curriculum design process follows a systematic four-stage workflow, referencing the figure above, ensuring quality control and adaptability to evolving technological trends. First of all is the lecture generation, weekly seminars are conducted with laboratory researchers, community developers, and university teachers to identify high-impact projects and translate them into lectures. These sessions produce hands-on tutorials, and lecture videos. The second step is lecture evaluation via learners’ feedback, all lectures are published on Bilibili.com, where learner engagement metrics (e.g., view counts, likes, comments) are monitored. Videos ranking in the top 30% of views and meeting predefined interaction thresholds (e.g., ≥ 5 comments per 500 views) proceed to formal review. The third step is expert review and lecture quality grading, a panel of instructors and industry experts evaluates shortlisted materials using a scoring rubric, referencing the table below. Criteria include technical accuracy, pedagogical structure, practical relevance, and experimental completeness. Courses scoring ≥ 80 are certified for integration into the formal curriculum. The last step is structured curriculum assembly, the approved courses are organized into tiered modules, spanning foundational concepts, intermediate programming topics, and advanced specializations (e.g., AI acceleration on RISC-V).

Criteria	Description
Technical Accuracy	Alignment with RISC-V specifications
Pedagogical Structure	Logical progression and clarity of content
Practical Relevance	Real-world application and hands-on utility
Experimental Completeness	Inclusion of lab exercises and assessments

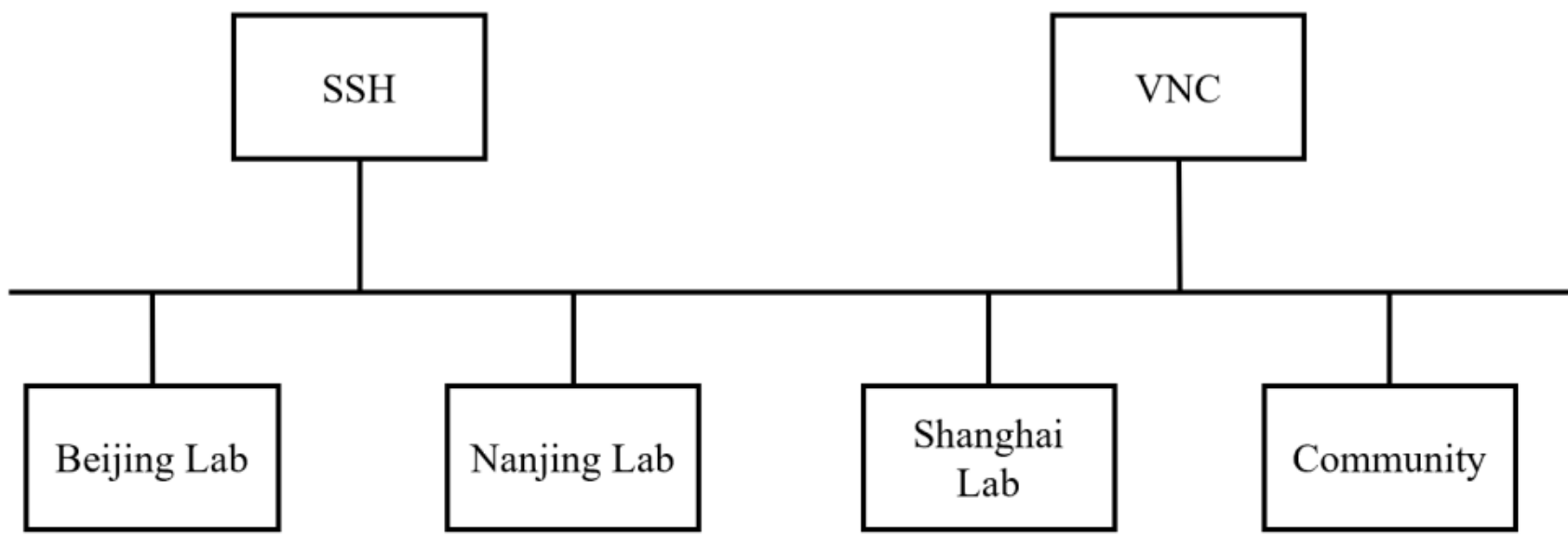


Community Engagement

To An essential part of our ecosystem is the cultivation of a vibrant, learner-driven community. With over 30,000 participants on Bilibili and WeChat, we host weekly livestreams, interactive Q&A sessions, and technical discussions. Offline events include hardware hackathons and a RISC-V programming competition that bridges learners with industry mentors.

Remote Laboratory Infrastructure

To overcome the physical limitations of hardware availability, we built a distributed remote laboratory environment spanning Beijing, Nanjing, and Shanghai. The lab integrates RISC-V boards such as the HiFive Unmatched and Licheepi4A, enabling access via SSH and VNC protocols. It supports remote firmware flashing through SD Mux and offers power control through smart outlets. A compatibility matrix has been developed to ensure seamless operation across multiple Linux distributions and RTOS platforms.



RISC-V Board and OS Support Matrix

Search board, cpu, core ...		Ruyidk Support
BananaPi BPI-F3 CPU: Key Stone K1 RAM: 2G/4G/8G/16G Core: SpacemiT X60	Lichee Cluster 4A CPU: TH1520 RAM: 8G/16G Core: XuanTie C910 + XuanTie C906 + XuanTie E902	Lichee Console 4A CPU: TH1520 RAM: 8G/16G Core: XuanTie C910 + XuanTie C906 + XuanTie E902
LicheePi 4A (16GB RAM) CPU: TH1520 RAM: 16G Core: XuanTie C910 + XuanTie C906 + XuanTie E902	LicheePi 4A (8GB RAM) CPU: TH1520 RAM: 8G Core: XuanTie C910 + XuanTie C906 + XuanTie E902	LicheeRV Nano CPU: SG2002 RAM: 2G Core: XuanTie C906 + ARM Cortex-A53
Milk-V Duo (256M) CPU: SG2002 RAM: 256MB Core: XuanTie C906 + ARM Cortex-A53	Milk-V Duo (64M) CPU: CV1800B RAM: 64MB Core: XuanTie C906	Milk-V Duo S CPU: SG2000 RAM: 256MB Core: XuanTie C906 + ARM Cortex-A53
LicheePi 4A (16GB RAM) CPU: TH1520 RAM: 16G Core: XuanTie C910 + XuanTie C906 + XuanTie E902	RevyOS @ LicheePi 4A (16GB RAM) Test Report System Version: 2023.03.1 Download Link: RevyOS@LicheePi4A Reference Installation Document: RevyOS@LicheePi4A	Test Environment System Information: - System Version: RevyOS 2023.03.1 - Download Link: RevyOS@LicheePi4A - Reference Installation Document: RevyOS@LicheePi4A Hardware Information: - LicheePi 4A (16GB RAM) + USB-A53 - USB-C to USB Adapter (PC Power Supply) - USB UART Debugger Installation Steps: Download and decompress image: Download the image, use "dd" to write it to the SD card. Flash to onboard eMMC via "fastboot" Use the fastboot to enter fastboot mode. Hold the BOOT button, then connect the USB-C cable to your PC on the other side to enter USB booting mode.
ArchLinux Version: 2023.01.14 Last Update: 2023-01-14	Armbian Version: 23.08.15 Last Update: 2023-01-04	Debian Version: 2023.01.04 Last Update: 2023-01-04
NeuOS Version: 2023.01.04 Last Update: 2023-01-04	RevyOS Version: 2023.03.1 Last Update: 2023-03-01	openEuler Version: 2023.03.1 Last Update: 2023-03-01

Results

To date, our Bilibili channels have published 859 educational videos, garnering over 1.33 million total views and nearly 39,000 likes. The main channel alone accounts for 748 videos, 1.29 million views, and 24,000 followers. Popular series include “RISC-V Software Porting and Optimization Championships,” “Hands-on RISC-V Simulator Tutorials,” and “Writing a RISC-V Compiler from Scratch.”

Metric	Primary Channel	Secondary Channel	Total
Number of Videos	748	111	859
Total Views	1.294 million	41,000	1,294,410
Total Likes	37,000	1,876	38,876
Total Followers	24,000	462	24,462

Incubated Projects

Understand RISC-V

<https://space.bilibili.com/1829697/channel/collectiondetail?sid=3467927>

Arduino on RISC-V Boards

<https://space.bilibili.com/1829697/channel/collectiondetail?sid=3744568>

WiringX on RISC-V Boards

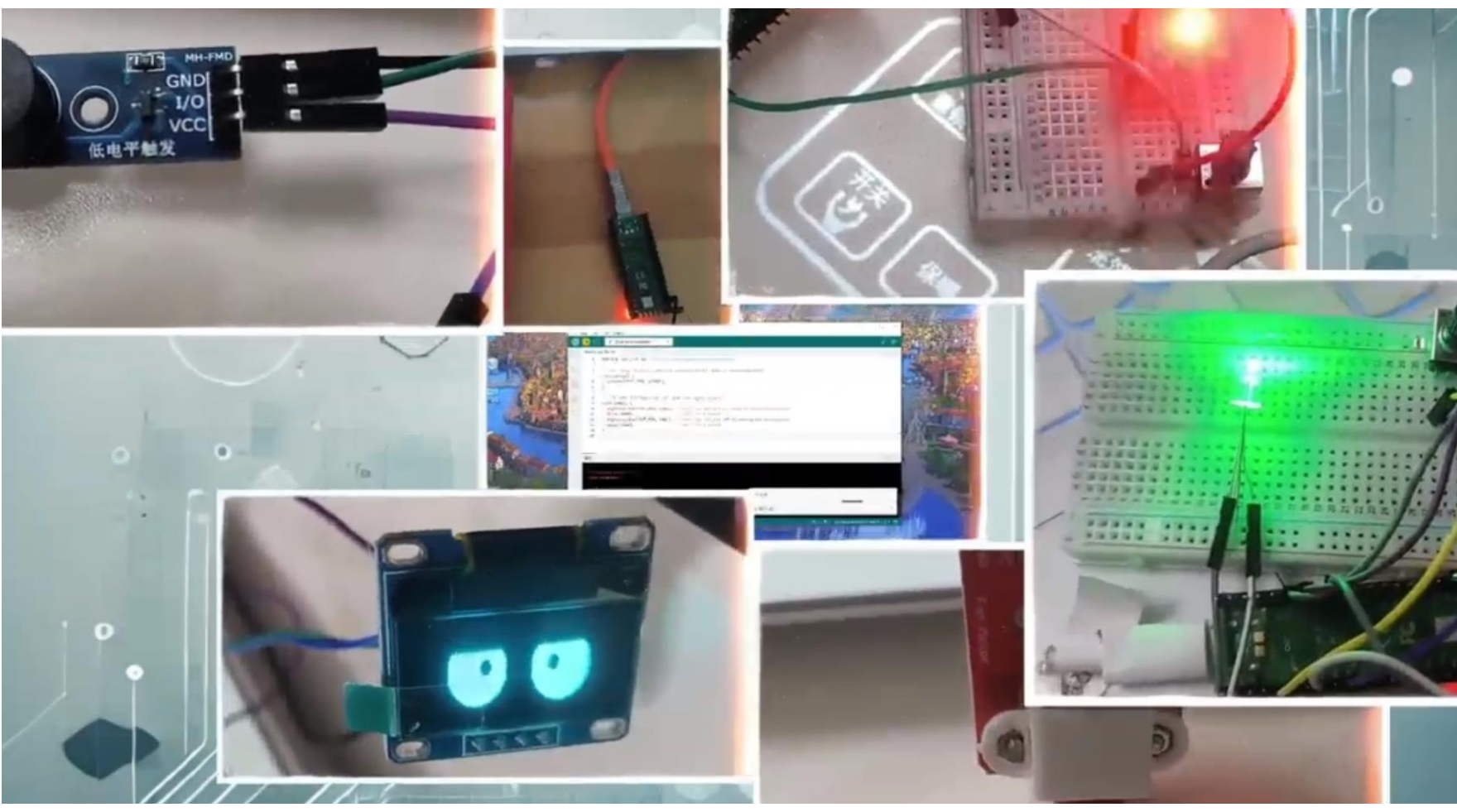
<https://space.bilibili.com/1829697/channel/collectiondetail?sid=4258135>

Floating Bridge for RISC-V Computing

<https://space.bilibili.com/1829697/channel/collectiondetail?sid=4096361>

YOLO on RISC-V Boards

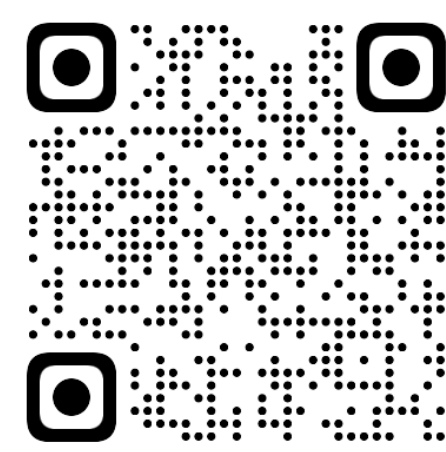
<https://space.bilibili.com/1829697/channel/collectiondetail?sid=5119595>



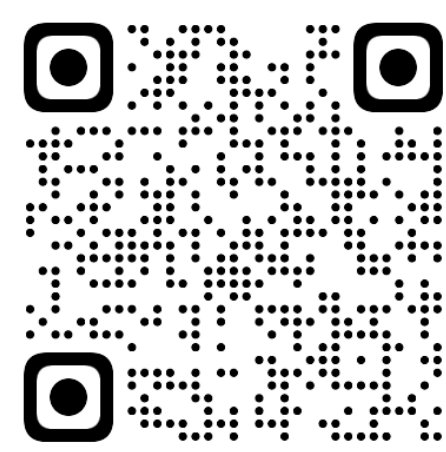
Conclusion

This initiative bridges the gap between RISC-V's technical potential and the practical need for scalable education. By combining structured curriculum pipelines, remote hardware access, and an active learner community, we offer a reproducible model for global RISC-V talent development. Our approach not only lowers the entry barrier for new learners but also accelerates innovation by enabling hands-on exploration of next-generation processor technologies.

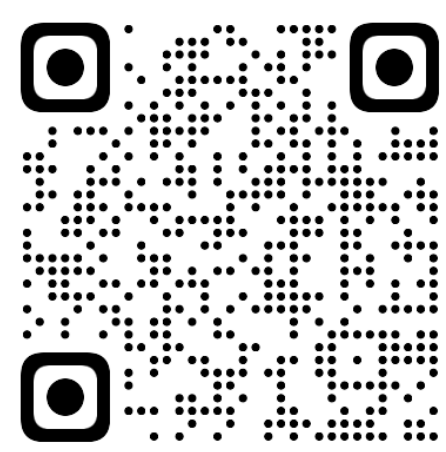
About Us



Bilibili
Channel 1



Bilibili
Channel 2



OS Matrix

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