# Learning by Puzzling: A Modular Approach to RISC-V Processor Design Education

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**Abstract**

*HADES-V is an innovative Open Educational Resource designed to teach RISC-V microcontroller design through a hands-on, modular approach. It consists of an extensive Instruction Guide document alongside an open-source template repository. This paper explores the didactic principles, technical foundation, and educational impact of HADES-V, emphasizing its open-source ethos and community contributions. We discuss the course design, evaluation framework, and student feedback, highlighting the jigsaw puzzle learning methodology with precompiled golden references. The work concludes with lessons learned and insights for future improvements and scalability in processor design education.*

## Introduction

Microcontroller and processor design is a cornerstone of modern engineering education, bridging theoretical concepts with practical hardware implementation. Traditional methods often fail to provide students with hands-on experience and real-world skills. HADES-V addresses these gaps by introducing a step-by-step approach to building a modular, pipelined 32-bit RISC-V processor. As an Open Educational Resource (OER), it empowers students and educators to explore processor design using open-source tools and methodologies.

As RISC-V is revolutionizing the hardware design landscape by promoting openness, customization, and accessibility, HADES-V leverages these principles to foster an inclusive and engaging learning environment. This paper outlines the didactical and technical aspects of HADES-V, evaluates its effectiveness through student feedback and educator insights, and discusses its potential to shape the future of processor design education. Introducing open-source practices into hardware design education addresses a crucial need for democratizing knowledge. Open standards such as RISC-V allow students and educators to freely explore and adapt the technology, promoting innovation and collaboration across academic and industrial domains. This democratization aligns with the core ethos of HADES-V, aiming to lower barriers and provide accessible, high-quality educational experiences.

The RISC-V Instruction Set Architecture (ISA) has gained traction for its simplicity, extensibility, and openness, making it ideal for educational purposes. Traditional teaching approaches to processor design often rely on abstract theoretical models or pre-built hardware, limiting student engagement and understanding. HADES-V bridges this gap by offering a framework that combines theoretical depth with practical application.

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Students design RISC-V microcontrollers using SystemVerilog, integrating hardware and software exercises for a holistic learning experience. The choice of tools like Verilator [1] and AMD Vivado [2] ensures that students are exposed to industry-grade software. The Basys3 FPGA board [3] serves as a practical platform for implementing designs, reinforcing the connection between theory and practice.

Educational innovations such as jigsaw puzzle pipelines and custom extensions in HADES-V allow students to experiment with processor architectures actively. This experimentation fosters solution-oriented thinking and creativity – essential skills in engineering. Additionally, the open-source nature of HADES-V ensures that its resources can be freely shared and adapted, encouraging collaboration and improvement within the educational community.

## The HADES-V Approach

The core didactic principle of HADES-V is the jigsaw puzzle methodology. Students implement each processor module individually, such as fetch, decode, execute, memory, and writeback stages. Precompiled golden references (supplied as Verilator libraries) can be used to validate their work, ensuring correctness without revealing the reference solution code. This approach fosters incremental learning and builds confidence. The entire digital design is created to be teachable rather than optimized.

The structured nature of the course enables students to understand complex systems by breaking them down into manageable components. Each module is designed to challenge students progressively, building on their previous knowledge and encouraging deeper engagement. The iterative validation process through golden references provides immediate feedback, helping students identify and correct errors effectively.

### Technical Foundation

HADES-V utilizes open-source tools like SystemVerilog for hardware description, Verilator and GTKWave [4] for simulation, and the industrial-grade AMD Vivado for the final FPGA synthesis. The Basys3 development board provides a tangible platform for implementing and testing designs. All resources, including the Instruction Guide [5] and the code template repository [6], are shared under CC BY 4.0 and MIT licenses, respectively, promoting global accessibility and adaptability. Educators can use a closed[1] test framework to rigorously assess the student's implementations. When supplying the output of the tests, this comprehensive evaluation system ensures that students develop a robust understanding of processor design principles while fostering a mindset of precision and reliability.

### Didactical Design

The HADES-V course is structured into progressive modules that can be developed individually and fit seamlessly into the architecture. Each module incorporates hands-on exercises that emphasize the practical application of theoretical concepts. Collaborative activities like peer reviews and group discussions foster shared learning. These activities enhance the educational experience by allowing students to learn from each other's insights and approaches. After completing all pipeline stages, assembling the microcontroller, and synthesizing it for the FPGA target, the final project allows students to showcase their creativity and technical expertise by developing unique features for their processors. The HADES-V Award, which is awarded to the best final projects, incentivizes excellence, encouraging students to push the boundaries of their learning.

## Evaluation and Feedback

HADES-V incorporates the extensive PERSEPHONE test framework, providing feedback to students and detailed performance insights and automated grading to educators. The framework ensures alignment with learning objectives while allowing students to identify and correct errors. This iterative process not only improves student outcomes but also enhances the course's overall quality.

Student feedback has been overwhelmingly positive. They appreciate the modular approach, real-world applicability, and the opportunity to work on open hardware. Examples of student projects include implementing games, custom ALU instructions, and optimizing memory access patterns. These projects demonstrate the course's ability to inspire innovation and practical problem-solving skills.

[1] To ensure students have no access to the reference implementation. Educators can request this framework with open, permissive license.

Educators have also benefited from the course's structured framework, which streamlines grading and provides valuable insights into student progress.

## Challenges and Lessons Learned

While HADES-V has been successfully launched, some challenges remain. The steep learning curve of digital system design tools and varying student familiarity with SystemVerilog require careful scaffolding. Balancing guided learning with fostering creativity is another critical aspect. Addressing these challenges involves extensive individual mentoring and developing supplementary materials, such as tutorials and walkthroughs, supporting students at different skill levels.

Future iterations of HADES-V aim to address these challenges by expanding the Instruction Guide and integrating new software tools that enhance the learning experience. These improvements will ensure that the course remains accessible and effective for a diverse and hopefully growing international student population.

## Conclusion and Future Work

HADES-V represents a paradigm shift in processor design education, combining open-source principles with innovative teaching methodologies. Its impact extends beyond the classroom, contributing to the global RISC-V and open hardware communities. HADES-V empowers students and educators to engage with cutting-edge technology by democratizing access to high-quality educational resources.

Future work includes expanding the framework with additional modules, tools, and hardware targets, creating online resources for remote learning, and fostering collaborations with other educational institutions. HADES-V hopefully continues to inspire and empower the next generation of digital design engineers by embracing openness and innovation.

## References


[1] Wilson Snyder. *Verilator*. URL: https://verilator.org/.

[2] Advanced Micro Devices, Inc. *Vivado Design Suite*. URL: https://www.xilinx.com/support/download.html.

[3] *Basys 3 Reference Manual*. Digilent, Inc. URL: https://reference.digilentinc.com/reference/programmable-logic/basys-3/reference-manual.

[4] Tony Bybell. *GTKWave*. URL: https://gtkwave.sourceforge.net/.

[5] Tobias Scheipel, David Beikircher, Florian Riedl. *Microcontroller Design, Lab: HaDes-V Instruction Guide*. URL: https://doi.org/10.3217/nytm4-grv34.

[6] Tobias Scheipel, David Beikircher, Florian Riedl. *HaDes-V Template Repository*. URL: https://github.com/tscheipel/HaDes-V.