One Student One Chip

Start From Scratch

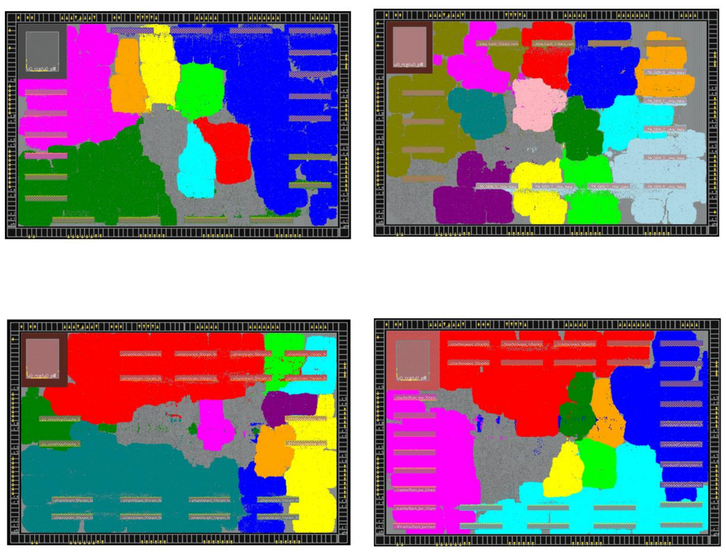
Create Your Own

RISC-V® Processor

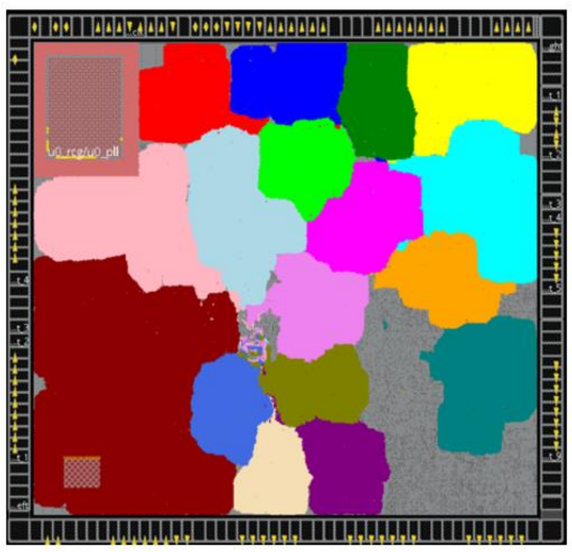
Website Overview

E-mail: ysyx@bosc.ac.cn

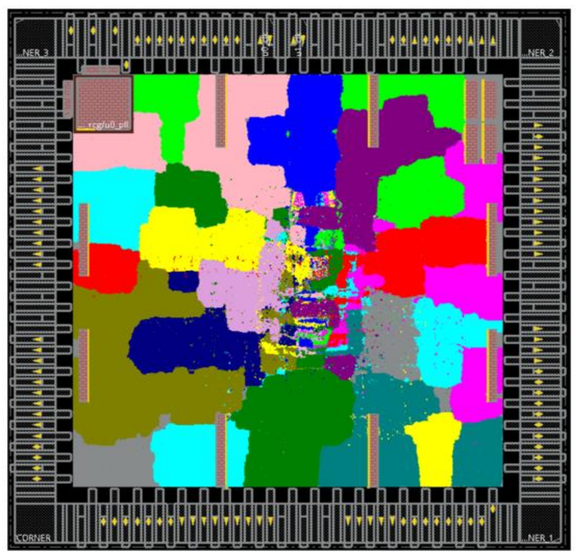
- Open Source and Free of Charge
- Over **11,000** Sign-Ups, Covering **900+** Universities
- SW-HW Co-design and Full Design Flow For Processor
- **No Enrollment Requirements**, Everyone is Welcome



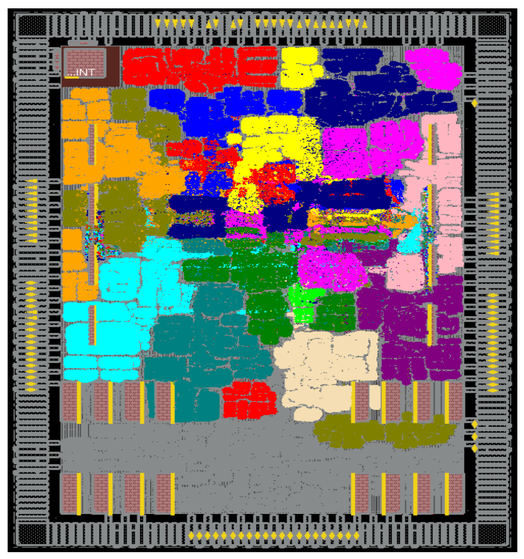
The 3rd Session of OSOC (1st Batch, 39 cores)



The 3rd Session of OSOC (2nd Batch, 9 cores)



The 4th Session of OSOC (1st Batch, 13 cores)



The 5th Session of OSOC (1st Batch, 13 cores)

Preliminary Stage

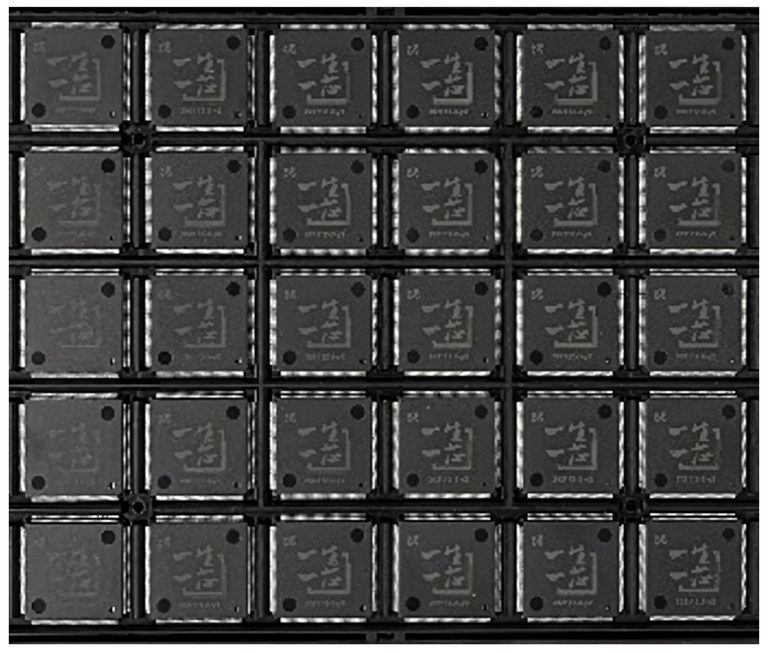
- GNU/Linux
- MakeFile
- Digital Circuit
- Verilog/Chisel
- Verilator
- C/C++
- Simulator

Basic Stage

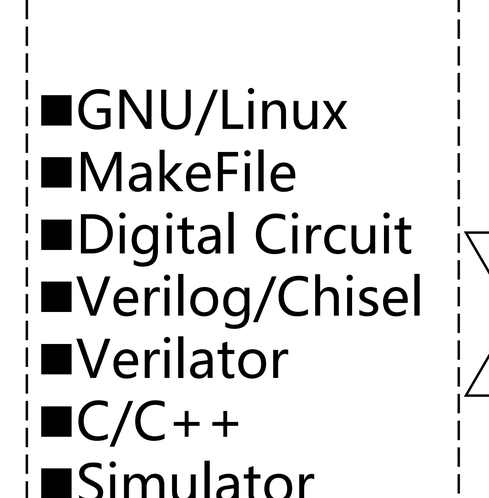
- Simulator
- Library Funcs
- Trace/DiffTest
- Single CPU
- Devices
- RT-Thread
- Benchmarks
- FC Games

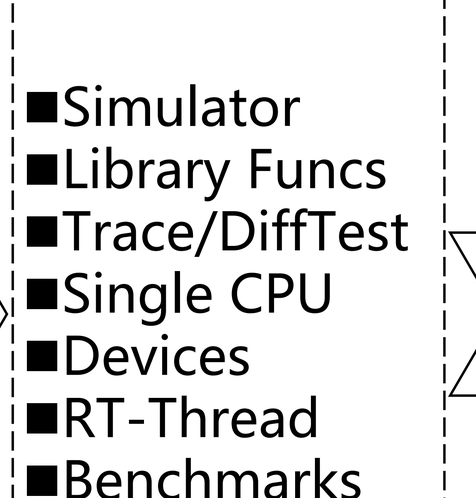
Advanced Stage

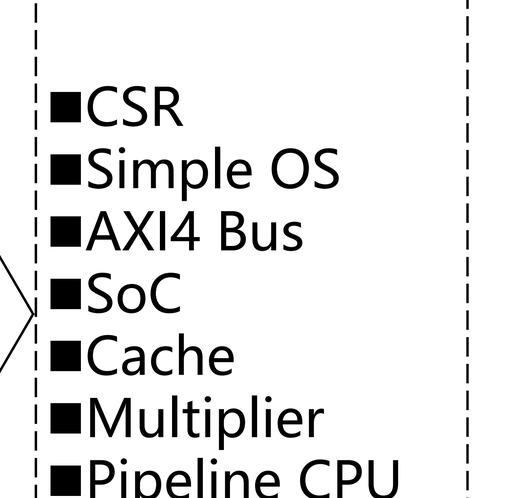
- CSR
- Simple OS
- AXI4 Bus
- SoC
- Cache
- Multiplier
- Pipeline CPU
- OS Games



Chips of OSOC







PCB Board Design&Testing