WebRISC-V: a 64-bit RISC-V Pipeline Simulator for Computer Architecture Classes

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Motivation

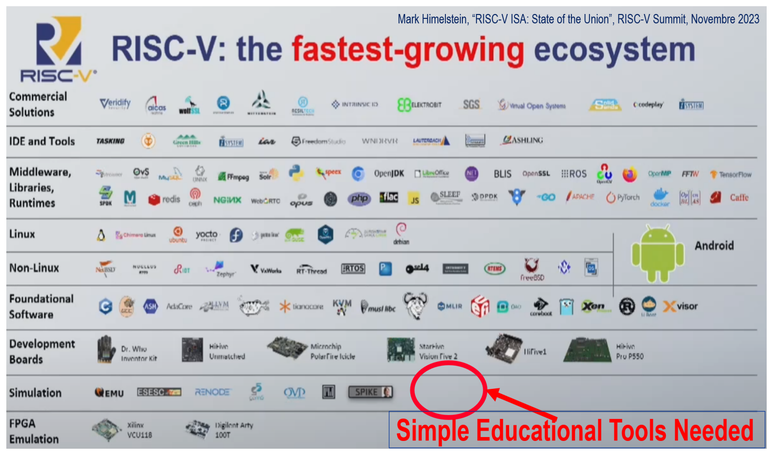
Contributing to the RISC-V acceptance in the Computer Architecture education communities by smoothing the migration from MIPS to RISC-V in classes, through the creation of a simple and easily accessible tool to test RISC-V programs on a pipelined processor

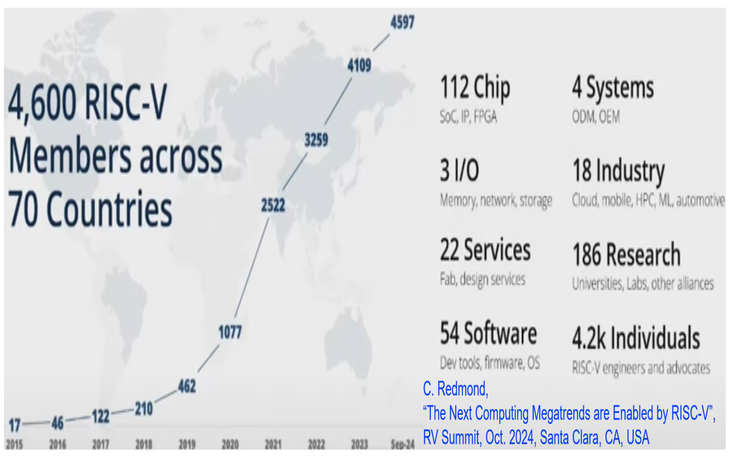
Achievements

- WebRISC-V is released as open source under the permissive BSD license [1]; it is possible to test it online at http://www.dii.unisi.it/~giorgi/WebRISC-V
- WebRISC-V was first presented in Phoenix, AZ, USA at the WCAE @ ISCA 2019, it is Open Access on the ACM digital library [2] and it continues to evolve!

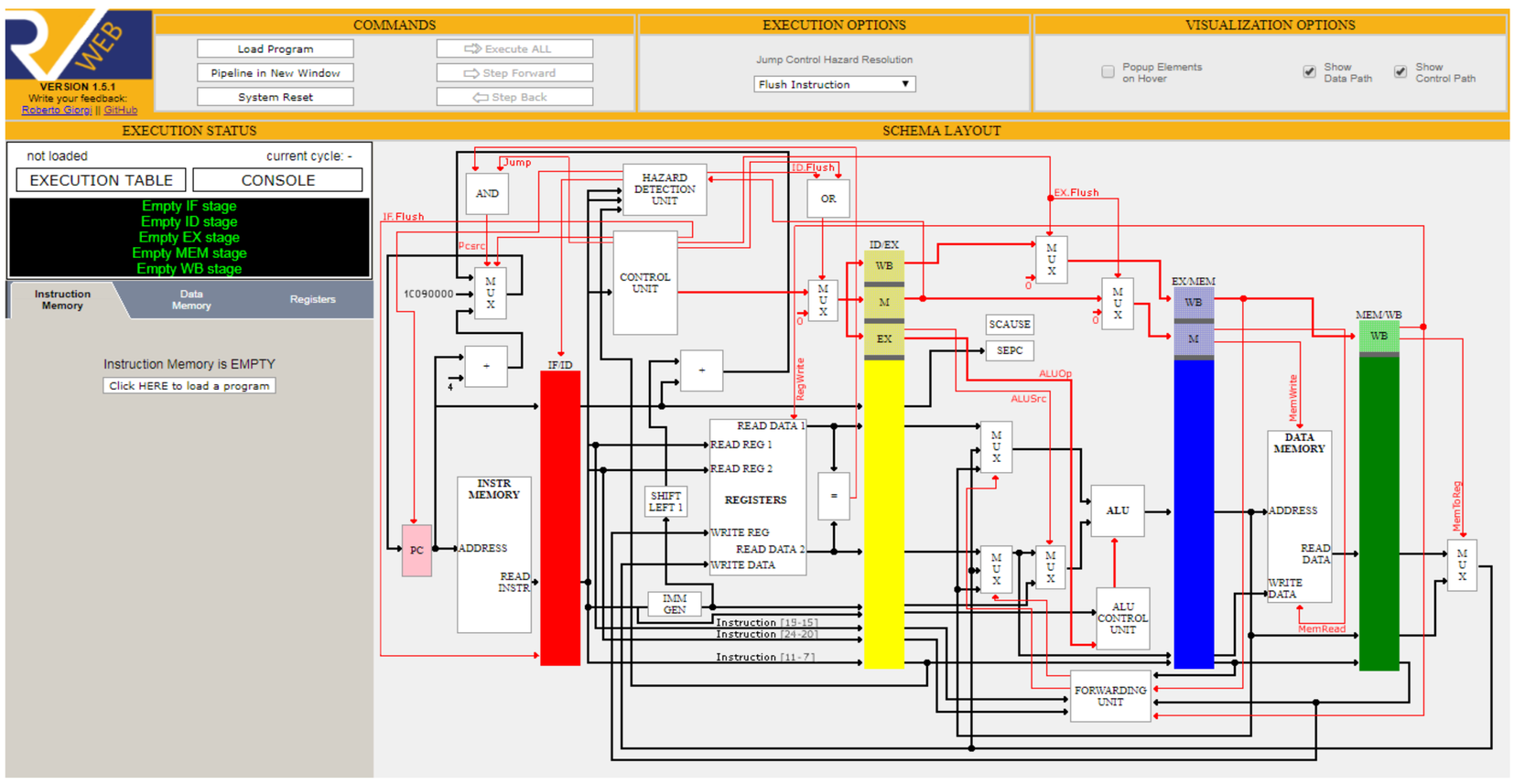
The need for RISC-V Educational Tools

- RISC-V is what Computer Architecture teachers are looking for: not tighten to a few vendors!
- It is open and the standard is maintained by the non-profit RISC-V Foundation [3]
- RISC-V educational tools are needed understand the sw/hw intricacies and basic concepts [4]





WebRISC-V



- WebRISC-V focuses on a subset of the ISA big enough for the execution of most common algorithms
- WebRISC-V is a 64-bit simulator: it implements the RV64I base part and the RV64M extension [5]

RV64I BASE INTEGER INSTRUCTIONS, in alphabetical order

MN.	FMT	NAME	MN.	FMT	NAME	MN.	FMT	NAME	MN.	FMT	NAME
add	R	ADD	lb	I	Load Byte	sll	R	Shift Left	sub	R	SUBtract
addi	I	ADD Immediate	lbu	I	Load Byte Unsigned	slli	I	Shift Left Immediate	sw	S	Store Word
and	R	AND	ld	I	Load Doubleword	slt	R	Set Less Than	xor	R	XOR
andi	I	AND Immediate	lh	I	Load Halfword	slti	I	Set Less Than Immediate	xori	I	XOR Immediate
beq	SB	Branch EQual	lw	I	Load Word	sltiu	I	Set < Immediate Unsigned	**RV64M Multiply Extension**		
bne	SB	Branch Not Equal	or	R	OR	sltu	R	Set Less Than Unsigned	mul	R	MULtiply
ebreak	I	Environment BREAK	ori	I	OR Immediate	sra	R	Shift Right Arithmetic	mulh	R	MULtiply High
ecall	I	Environment CALL	sb	S	Store Byte	srai	I	Shift Right Arith Imm	div	R	DIVide
jal	UJ	Jump & Link	sd	S	Store Doubleword	srl	R	Shift Right	rem	R	REMainder
jalr	I	Jump & Link Register	sh	S	Store Halfword	srli	I	Shift Right Immediate			

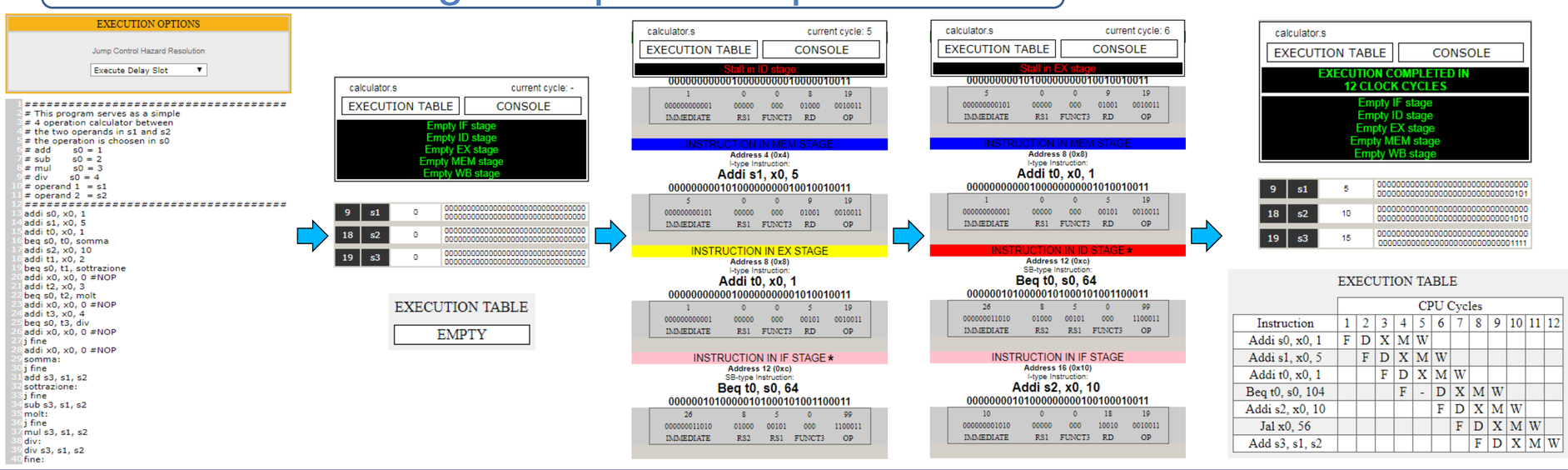
Comparison with other Datapath simulators

WebRISC-V was compared with several Datapath simulators of several architectures: WinDLX [6] of DLX, MARS MIPS X-Ray [7], DrMIPS [8], Mipster32 [9], UCOMIPSIM [10], Visimips [11], WASP [12], WebMIPS [13] of MIPS and Ripes [14] of RISC-V.
The following table was produced from this process.

		Graphical Presentation	Visualization Architectural Elements	Datapath Implementation		Web Accessibility	
				syngle cycle	pipelined	client side[1]	server side[2]
DLX	WINDLX	Stage Blocks			✓		
MIPS	MARS X-RAY	Datapath		✓			
	DrMIPS	Datapath with Control Unit	✓	✓	✓		
	Mipster32	Stage Blocks			✓		
	UCOMIPSIM	Datapath with Control Unit	✓		✓		
	Visimips	Datapath with Control Unit			✓		
	WASP	Datapath with Control Unit	✓		✓	✓	
	WebMIPS	Datapath with Control Unit	✓		✓		✓
RISC-V	RIPES	Datapath			✓		
	WebRISC-V	Datapath with Control Unit	✓		✓		✓

[1] Additional plug-ins required.
[2] Accessible directly from the Web without the use of plug-ins.

Executing a simple example



EXECUTION TABLE

Instruction	CPU Cycles										
	1	2	3	4	5	6	7	8	9	10	11	12
Addi s0, x0, 1	F	D	X	M	W							
Addi s1, x0, 5		F	D	X	M	W						
Addi t0, x0, 1			F	D	X	M	W					
Beq t0, s0, 104				F	-	D	X	M	W			
Addi s2, x0, 10						F	D	X	M	W		
Jal x0, 56							F	D	X	M	W	
Add s3, s1, s2								F	D	X	M	W

Here we can see some snippets of an execution, with the Delay Slot activated, of the example code "Simple Calculator".
We can see the occurrence and passing through the pipeline of stalls and the instructions that generated them, what happens in the registers and the clock cycles necessary for the code provided.

References

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Acknowledgements

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