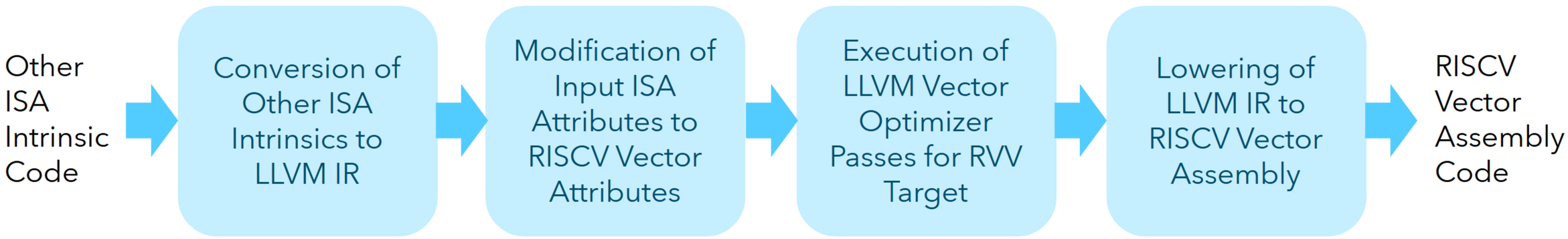
Auto-Transcode

into RISCV Vector Code from Other Vector/ SIMD ISAs using LLVM Infrastructure

(Quickly Bring-up Optimized Libraries and Workloads on RISCV Vector and Other Architectires)

- Auto Re-Vectorization Flow



- General Compilation Flow

Example Result with Matmul Kernel

Target Processor	Generic Flow (cycles)	Auto Re-Vectorization Flow (cycles)	Performance Gain
SiFive X280	548	315	1.74 x
SiFive P670	91	52	1.75 x

- Quickly bring up optimized libraries and workloads on processors with new architectures like RVV1.0 (reduces manual effort)
- Can be a more efficient starting point for further hand-optimization
- Modular design - leverages LLVM infrastructure - so can be extended to any input and output ISAs supported in the LLVM ecosystem
- Plans to open-source the tool

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