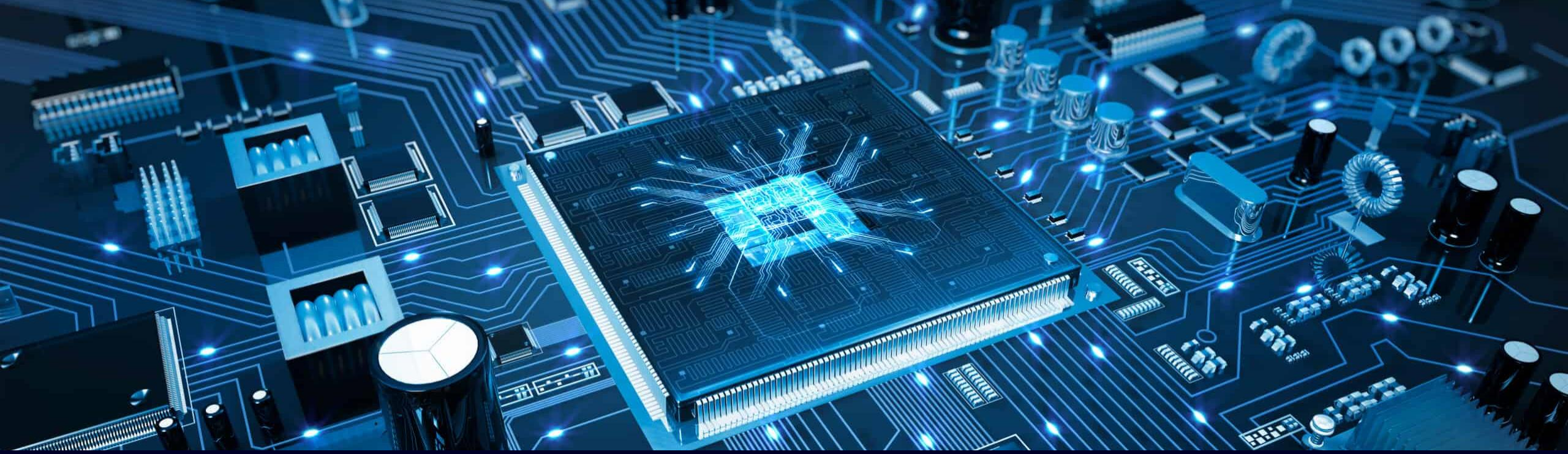

Efficient Debug and Trace of RISC-V Systems: a hardware/software co-design approach

Oana Lazar, Embedded Software Engineer, Tessent Embedded Analytics

RISC-V Summit Europe, 15th May 2025

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Agenda

Hardware/software co-design approach

Highly efficient trace

Minimally intrusive logging of program flow

Harnessing hardware/software benefits

System integration verification for an end-to-end debug and trace solution

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Increased complexity brings increasingly complex issues

1 System complexity

- Generative AI
- High-performance computing
- Multi-chiplet technologies

2 Bug complexity

- Silent Data Corruption & Heisenbugs
- Existing solutions interfere with sensitive bugs
- More in-depth visibility is needed

3 Skills shortage

- Non-intrusive solutions to facilitate debugging
- More visibility for multiple debug methods and insights
- Minimize ramp-up: use existing freeware & open-source solutions

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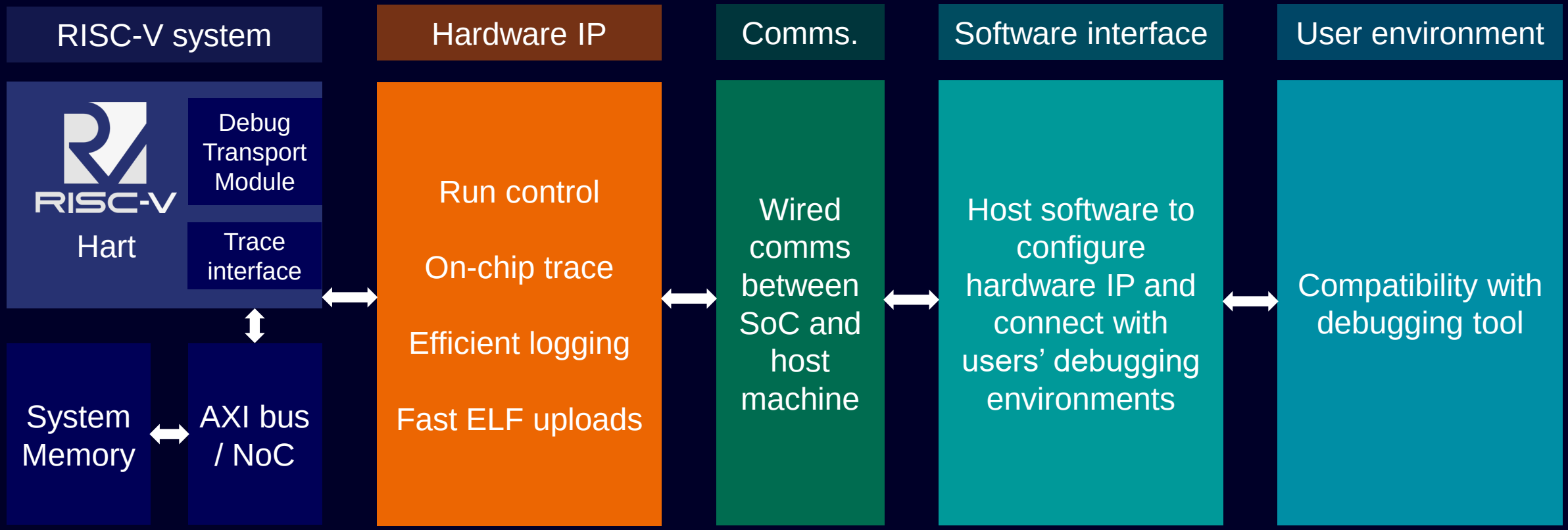
Hardware/software co-design approach

Designing the hardware with software in mind, and vice-versa



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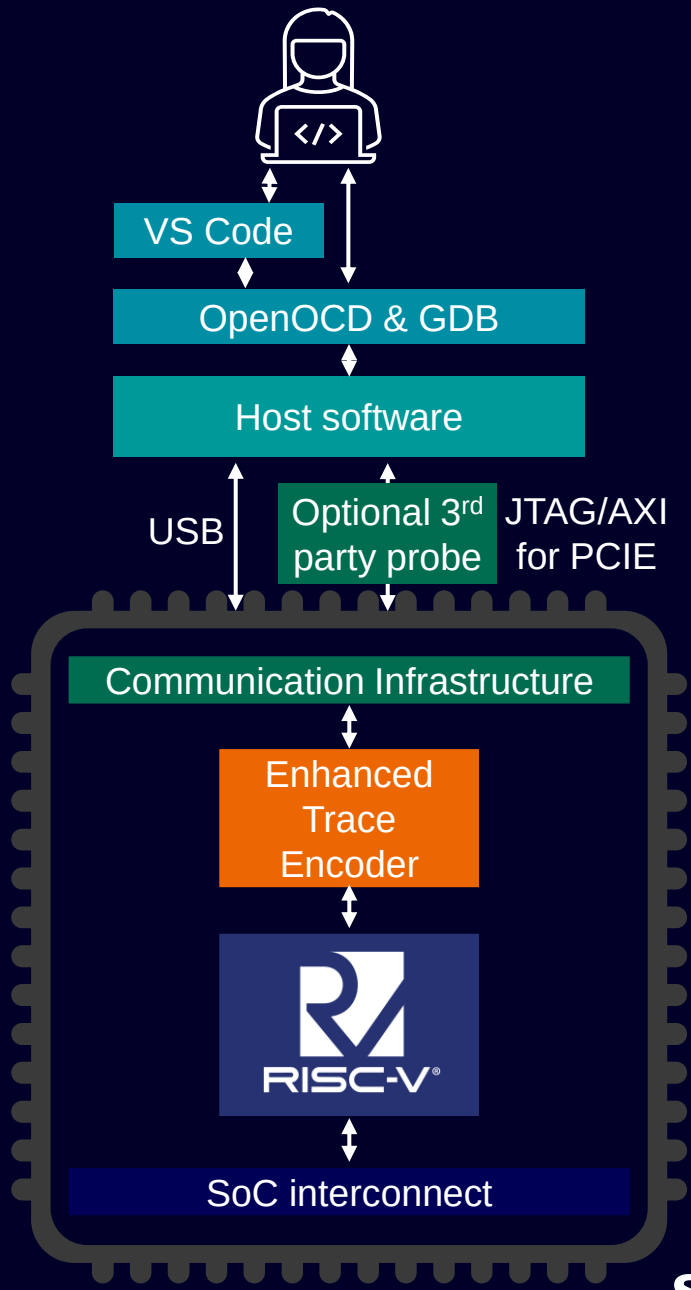
Highly efficient trace

Trace decoding and reconstruction:

- Performed out-of-box with GDB
- Custom instructions support
- Filtering options

Trace generation:

- Fully compliant with the ratified “Efficient Trace for RISC-V (E-Trace)” specification
- Complex systems under heavy wo
  lot of trace – high compression is c
- Optional hardware extensions avai
  compression rates
- Average compression rate of 0.231
  with no extensions enabled



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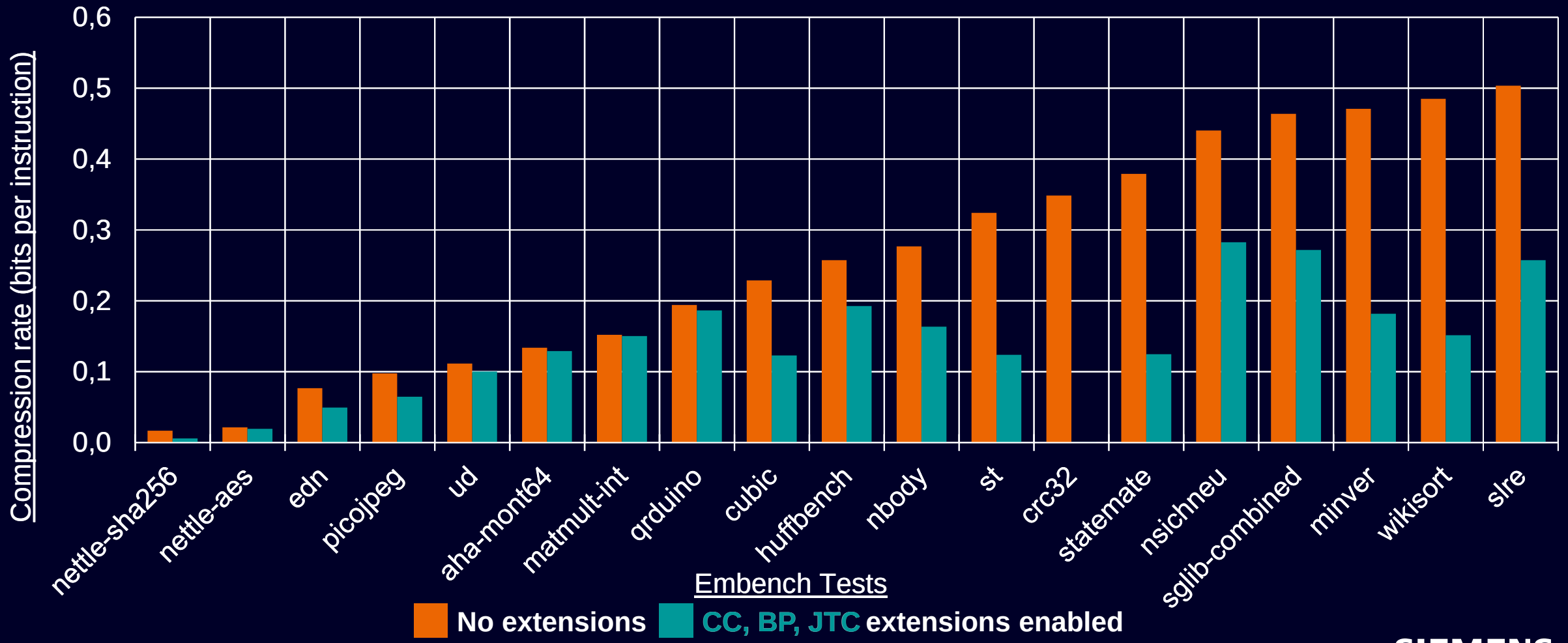
Highly efficient trace

Embench™ Benchmark results show ~40% compression rate improvement with optional extensions



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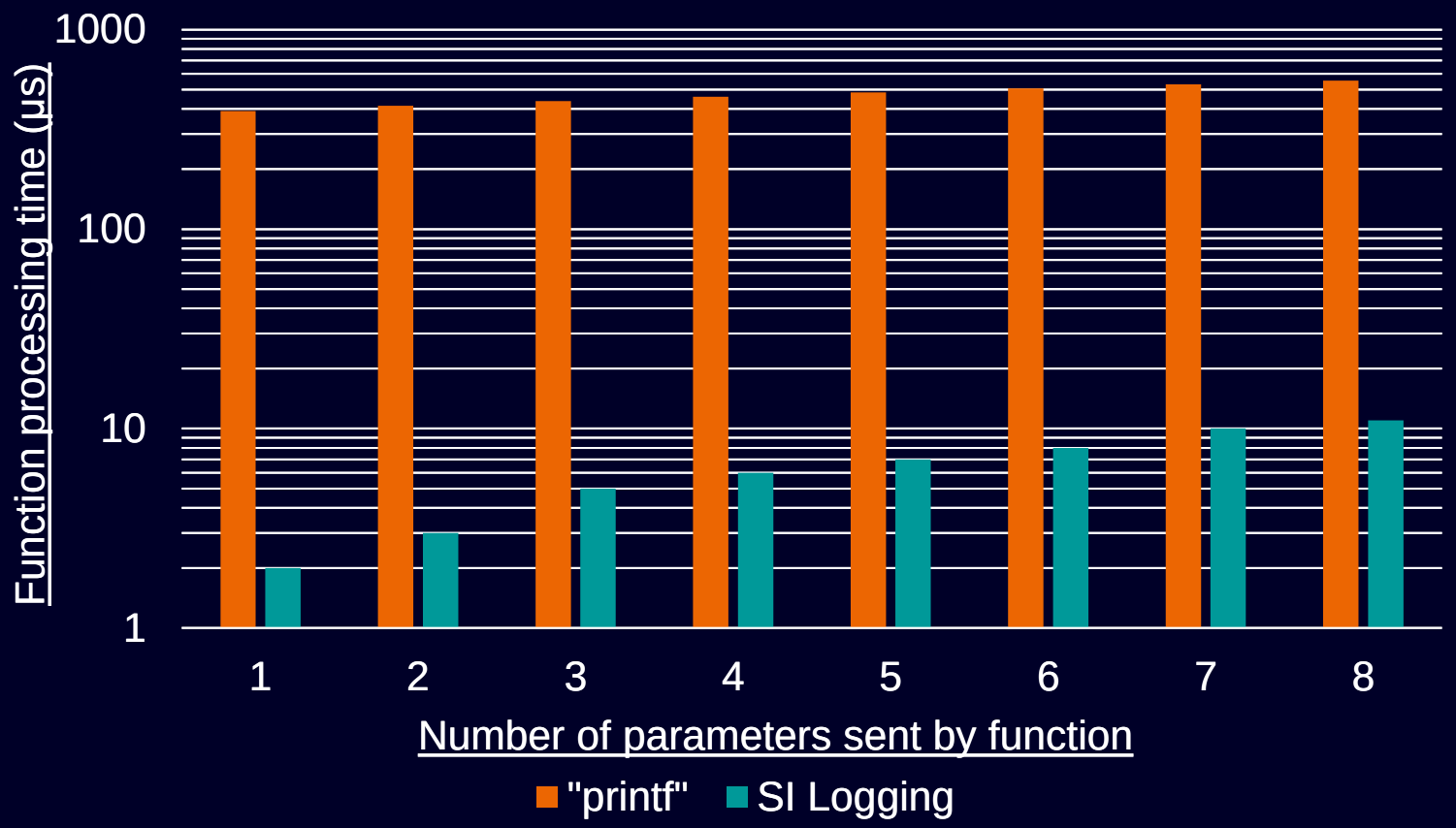
Minimally intrusive logging of program flow

Static Instrumentation Module provides:

- Minimally intrusive logging via an intuitive “printf”-like API
- SI logging which only takes 0.2-0.3% of the processing time “printf” equivalents take to run
- Minimal interference with program flow, accelerating debug of timing-sensitive Heisenbugs




```
UST_LOGGING_DEBUG_PARAM3(“Pixel write y=%d, x=%d,
                         colour=%u”, y, x, colour);
```

With contributions from:
Rod Boyce, Principal Software Engineer, Tessent Embedded Analytics
Luke Southwell, Senior Software Engineer, Tessent Embedded Analytics

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Harnessing hardware/software benefits

Direct Memory Access Module

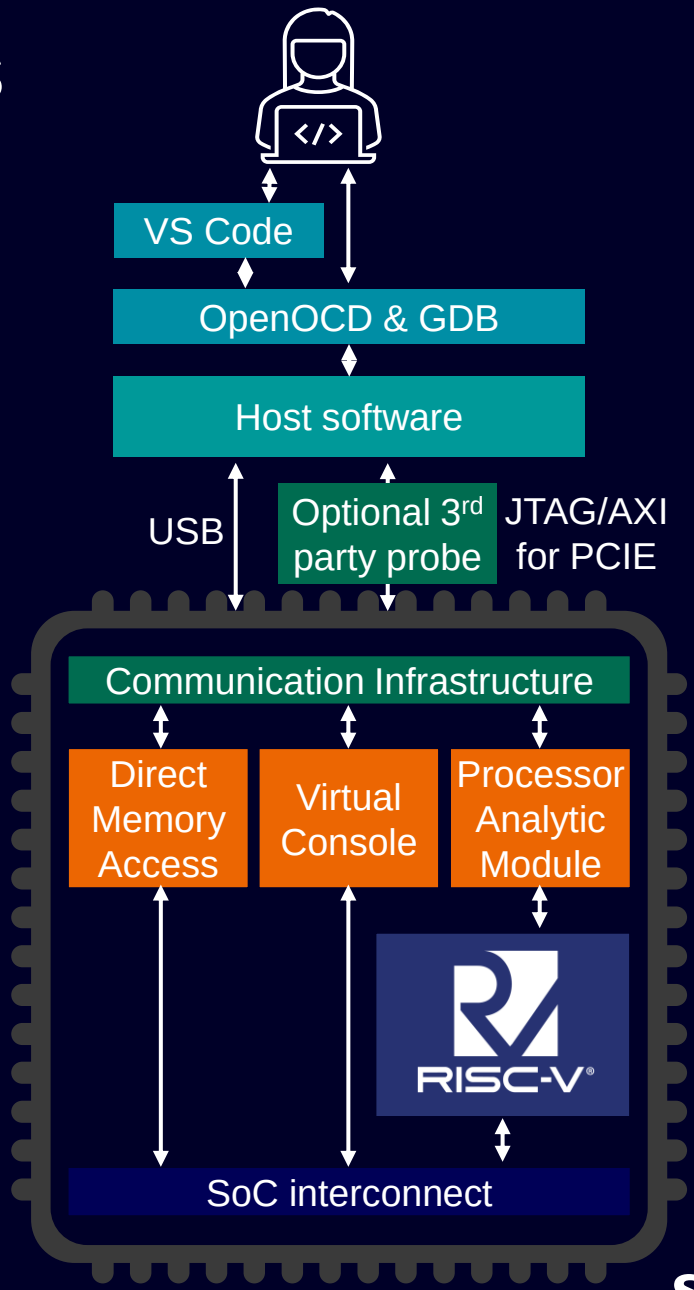
- Speed-up of 100x over software-only solutions for on-chip ELF file uploads

Virtual Console Module

- Multiple “virtual” bi-directional off-chip communication channels, with no added pins

Processor Analytic Module

- Debug access to multiple RISC-V harts via a single wired connection



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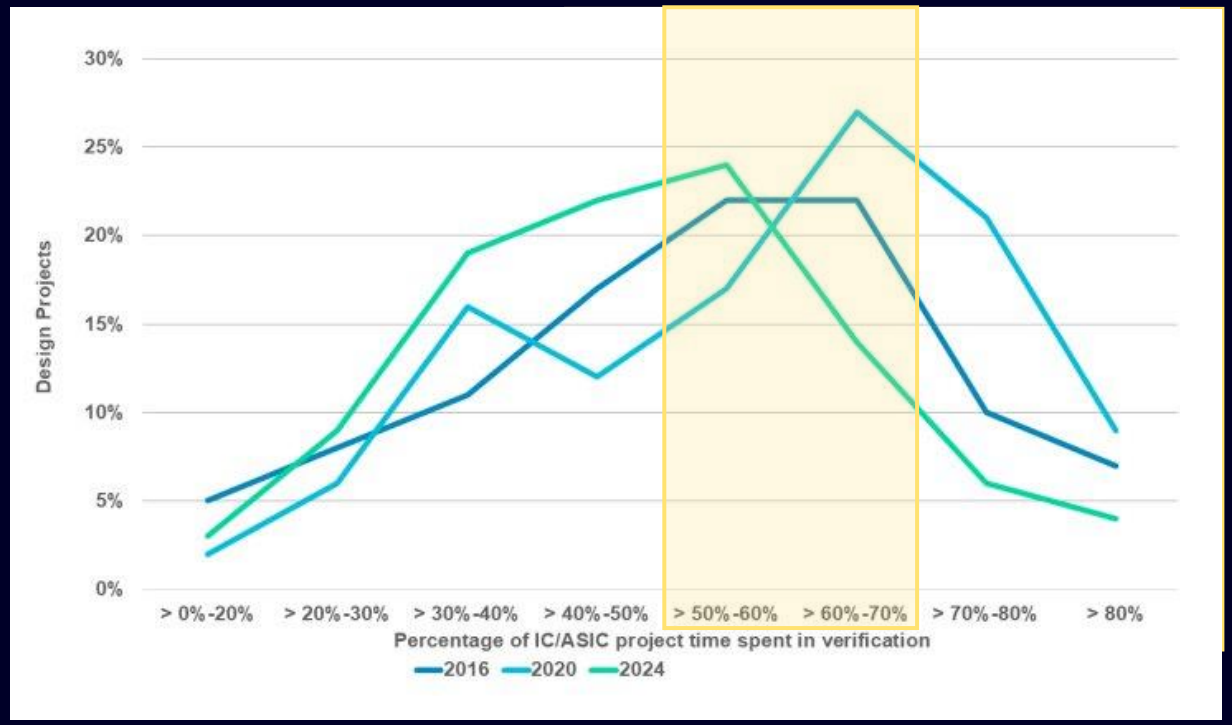
System integration verification



"Projects spending minimal time typically reuse pre-verified IP modules, reducing verification overhead."

"Conversely, projects with **significant verification time** often involve **high proportions of newly developed IP**"

2024 Wilson Research Group IC/ASIC functional verification trend report

Mean ASIC project time spent in verification: ~50%

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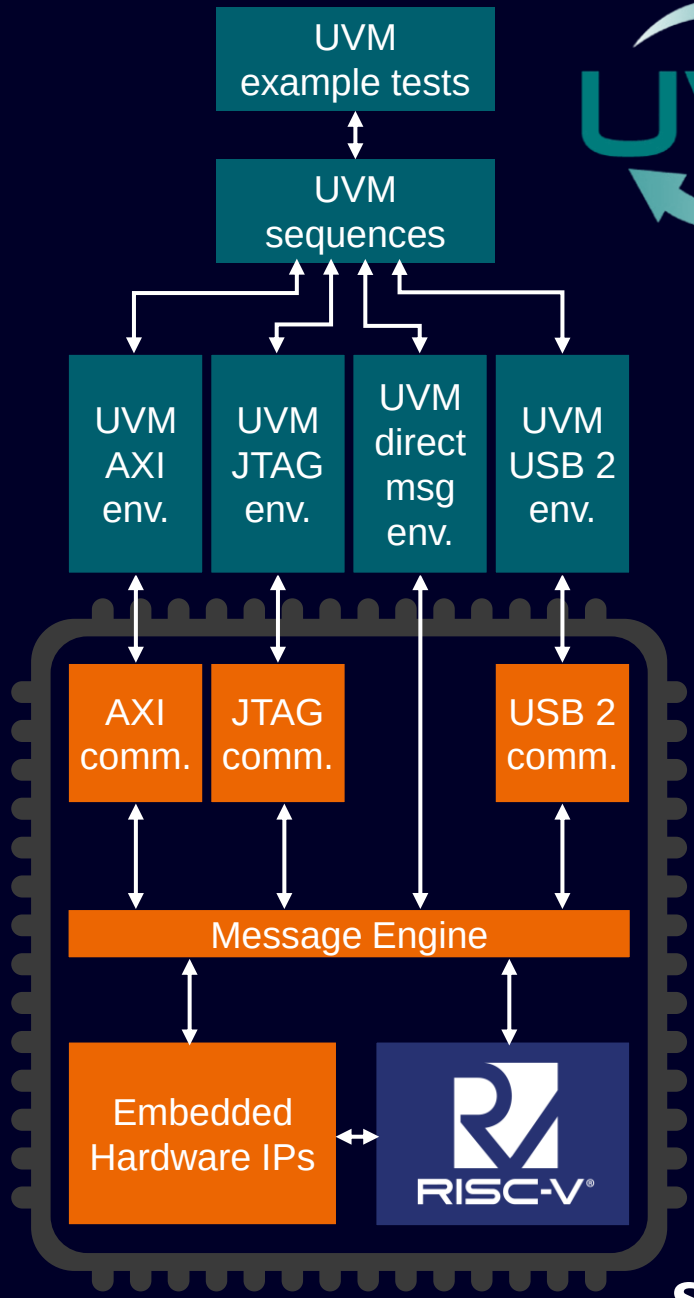
System integration verification

Verifying system integration of pre-verified IPs:

- Ensures that verified IPs are correctly connected to each other and system components
- UVM integration environment with virtual interfaces for each communicator IP
- UVM-based environment leverages its reusability and verification capabilities



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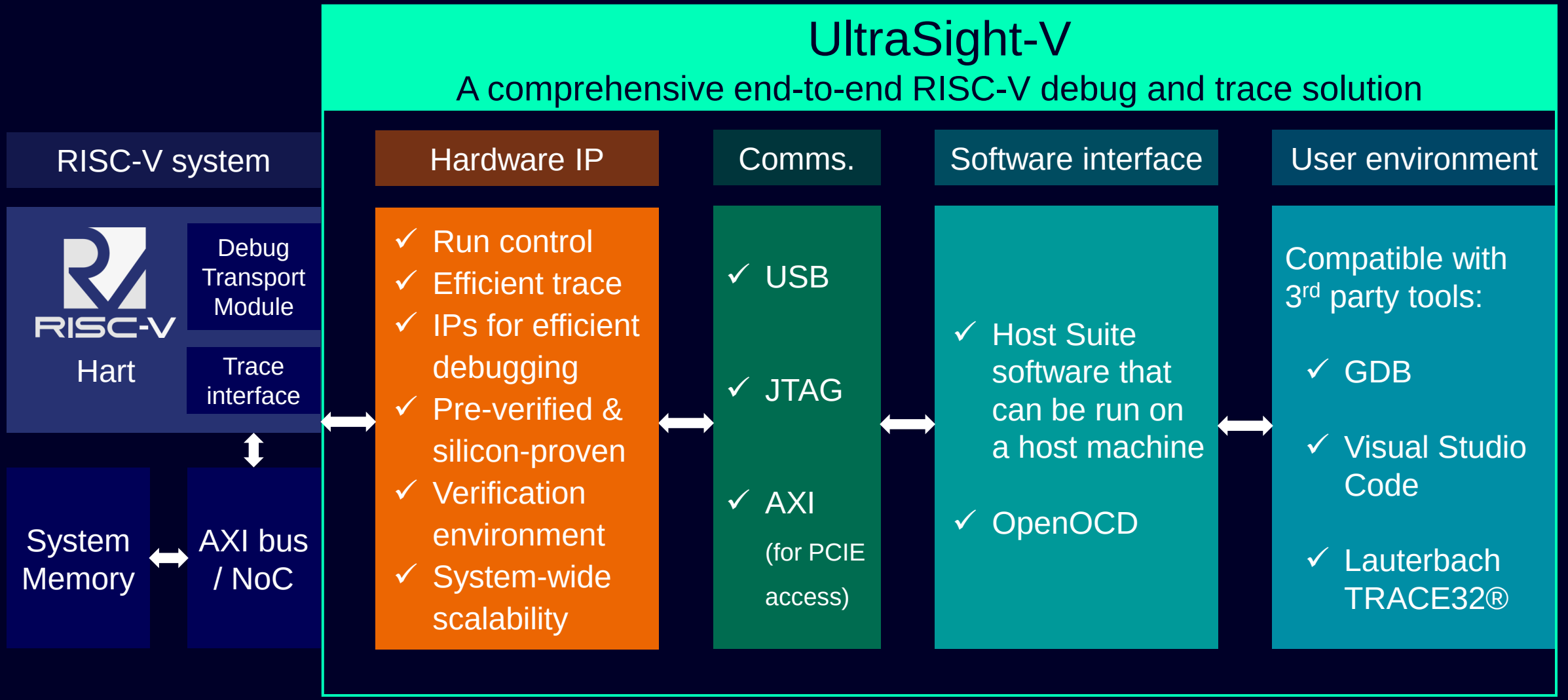
Tessent UltraSight-V



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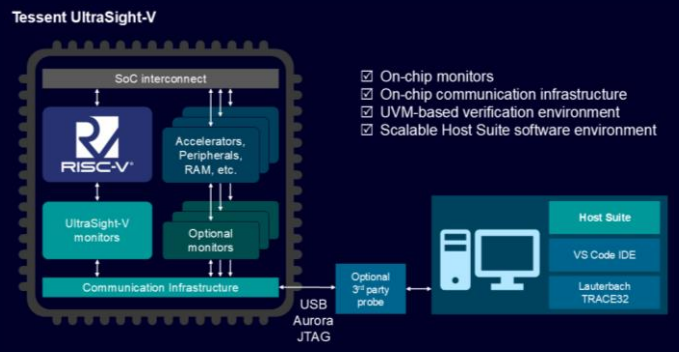
Visit us at Booth #30

Join us at RISC-V Europe Summit 2025

Demo presentation

RISC-V on-chip debug & trace solution: Tessent UltraSight-V

Tuesday May 13, 15:55



Keynote Presentation

Enhancing your RISC-V SoC debug & optimization with embedded functional monitors

Wednesday May 14, 09:30

*Recording will be made available

Presentation

Unleashing the Power of RISC-V E-Trace with a Highly Efficient Software Decoder

Thursday May 15, 11:45

*Poster on display during the Summit

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