

# RISC-V: Reaching New Orbits in Space Computing

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### RISC-V is flying in space



- TRISAT-R, Nanosatellite by Skylabs/University of Maribor (SI), launched July 2022
- Polarfire-SoC with RISC-V subsystem on the ISS in 2022 (SpaceBilt)
- HARV RISC-V SoC on ROBUSTA-3A, launched 2024
- Al-eXpress, launched Jan 2025
- ETHZ Trikarenos, 15<sup>th</sup> March 2025









### Space specific technical constraints



### Reliability

#### Radiation

- Total ionising dose (TID) and single event effects (SEU)
- Commercial off-the-shelf (COTS) → needs expensive testing and system level mitigation
- Radiation hardening by design (RHBD), redundancy

#### Vacuum

Outgassing from package materials → contamination of sensors

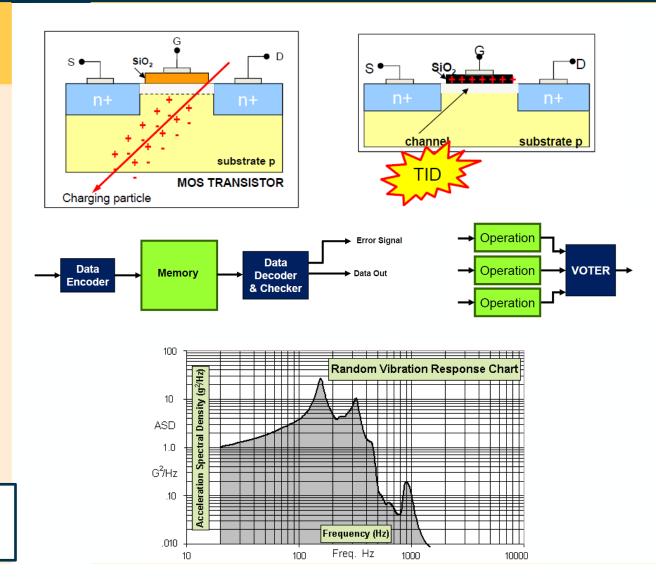
#### Vibration

At launch → stress on interconnects

#### Temperature

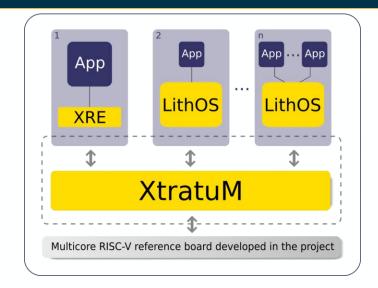
Satellites can be very hot and very cold (-55 to 125 deg C) → challenge for timing closure.

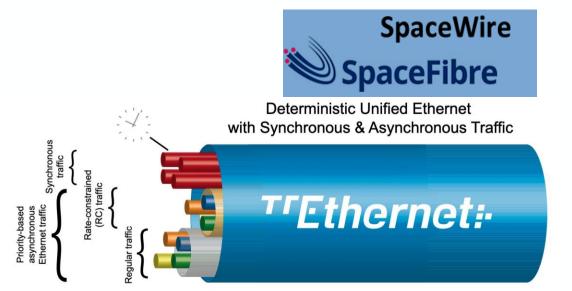
Lifetime of satellites up to 20 years longer than commercial electronics → No repair!



### Space specific technical constraints







#### **Functional**

#### Determinism

Needed by timing critical control functions (launch, landers)

#### Mixed criticality software

 Different levels of trust, time and space partitioning for fault containment.

#### Specific interfaces

- Often inherited from commercial, automotive or military standards with additional constraints (determinism, electrical environment).
  - MIL-1553B (galvanic isolation, inherited from aeronautics)
  - SpaceWire (derived from IEEE1355 D/S encoding)
  - SpaceFibre (extension of SpaceWire to high speed SerDes)
  - Time Sensitive Networking (TSN) / TimeTriggered-Ethernet (TTE)

### Economic and organisational constraints in space



#### Low recurrent part count: main cost drivers: design, CAD and mask (not silicon area)

- Custom project ASIC for a few or 10s of parts in one-off satellite.
- Successful space standard product can reach 1K or 10K parts shipped.

#### Long product life cycles: 10 years development, 10 years sales, 10 years in orbit

• Obsolence issues: tenchnology, engineers, companies

#### Expensive supply chain: ceramic hermetic package, leaded interconnect, solder columns...

- Space qualification batch → destructive testing (50-100 flight parts)
- Recurrent prices dominated by packaging, assembly, testing, screening (not silicon area)
- Price per space-qualified part can be > 50KEuro (commercial part 1– 100\$)

#### **Attracting commercial players**

- Foundry backend services only support high volume products (e.g. TSMC 12 Million wafers/year; our projects 12 wafers).
- Revenue from IP royalties from space use come too late → increased license fees.

### Public funding: dependency on political decisions

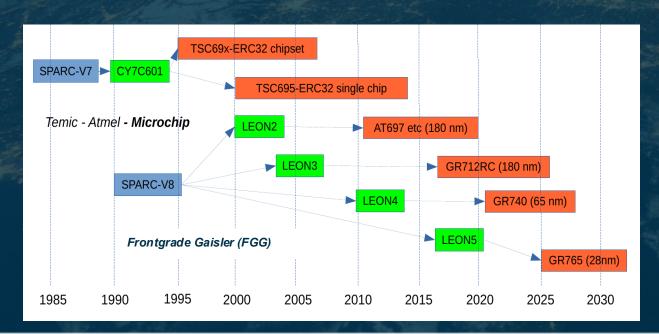
- Multiple funding organizations and schemes: ESA, national bodies, EC, ...
- Spending rules: geographical return, consortium composition (LSI, SME, academia)

### Importance of open ISA – Going for RISC-V



- Non-dependence: multiple IP sources, or own development.
- Free and open standard, allowing for customization.
- Easier to modify for radiation hardening when compared with proprietary ISA.
- Industry and academia in the game: commercial and open source.
- Stable specification, low complexity, GNU tool chain.

Open ISA allows for competition of multiple IP sources → warrants for flexibility and non-dependence



SPARC in space success story
25 years
5 generations

SPARC is in all our missions
Europe, US, China, Japan
with > 20000 flight parts
standard processors
SPARC IP in FPGA
mature SW ecosystem
demand in space continues

## Importance of open ISA – RISC-V is taking over



Huge and growing developer's community.

Open hardware community.



Workshop April 2-3, 2025 | Gothenburg

2022 -> 70

2025 -> 180 attendees



RISC-V中国峰会

2024

# Importance of open ISA – RISC-V is taking over



Huge and growing developer's community.

Open hardware community.

| Name                          | Stars <b>▼</b> | Forks | Liconeo      | Commits in the last year | Latest commit in the last year | Comment                                   |
|-------------------------------|----------------|-------|--------------|--------------------------|--------------------------------|---|
| OpenXiangShan/XiangShan       | 4700           |       |              | >30                      |                                |   |
|                               | 3200           | 1100  |              | >30                      |                                |   |
| chipsalliance/rocket-chip     | 3200           |       | ISC          | >30<br>10                |                                |   |
| YosysHQ/picorv32              |                |       |              |                          |                                |   |
| SpinalHDL/VexRiscv            | 2400           |       | MIT          | >30                      |                                |   |
| openhwgroup/cva6              | 2200           | 673   |              | >30                      |                                |   |
| darklife/darkriscv            | 2100           |       | BSD-3-Clause | >30                      |                                |   |
| riscv-boom/riscv-boom         | 1700           |       | BSD-3-Clause | >30                      | ,                              |   |
| stnolting/neorv32             | 1600           |       | BSD-3-Clause | >30                      |                                |   |
| olofk/serv                    | 1400           |       | ISC          | >30                      |                                |   |
| OSCPU/NutShell                | 1400           |       |              | >30                      |                                |   |
| lowRISC/ibex                  | 1300           |       | Apache-2.0   | >30                      |                                |   |
| ZipCPU/zipcpu                 | 1300           | 153   |              | 9                        | 20,00,202                      |   |
| riscv-mcu/e203_hbirdv2        | 1200           |       | Apache-2.0   | 1                        | 05/09/2024                     |   |
| vortexgpgpu/vortex            | 1200           |       | Apache-2.0   | >30                      |                                |   |
| rsd-devel/rsd                 | 978            |       | Apache-2.0   | >30                      |                                |   |
| syntacore/scr1                | 842            | 268   |              | 3                        | 26/09/2024                     |   |
| eugene-tarassov/vivado-risc-v | 821            | 187   |              | 29                       | 22/09/2024                     |   |
| hughperkins/VeriGPU           | 778            | 89    | MIT          | 4                        | 21/06/2024                     |   |
| splinedrive/kianRiscV         | 689            |       | ISC          | >30                      | 19/09/2024                     | Project intended as a demonstrato         |
| PrincetonUniversity/openpiton | 627            | 212   |              | 5                        |                                | Can use the 64-bit CVA6, but no license   |
| sergeykhbr/riscv_vhdl         | 619            | 102   | Apache-2.0   | >30                      |                                | 64-bit CPL                                |
| black-parrot/black-parrot     | 599            | 178   | BSD-3-Clause | >30                      | 23/09/2024                     | 4 64-bit CPL                              |
| ucb-bar/riscv-mini            | 538            | 110   |              | 2                        | 03/06/2024                     | Project intended as a demonstrato         |
| riscv-non-isa/riscv-arch-test | 502            | 191   | Apache-2.0   | >30                      | 23/09/2024                     | Not a RISC-V CPU                          |
| openhwgroup/core-v-verif      | 427            | 218   |              | >30                      | 24/09/2024                     | Not a RISC-V CPU                          |
| bluespec/Flute                | 351            | 55    | Apache-2.0   | 1                        | 19/10/2023                     | 32-bit or 64-bit CPU, written in Bluespec |
| minerva-cpu/minerva           | 301            | 32    |              | 6                        | 24/09/2024                     |   |
| RoaLogic/RV12                 | 282            | 50    |              | 11                       | 08/06/2024                     | Non-Commercial License                    |
| skordal/potato                | 260            | 41    | BSD-3-Clause | 1                        | 19/08/2024                     | 32-bit CPU                                |
| SpinalHDL/NaxRiscv            | 258            | 39    |              | >30                      | 23/09/2024                     | 32-bit or 64-bit CPU written in SpinalHDI |
| standardsemiconductor/lion    | 248            | 16    | BSD-3-Clause | >30                      | 02/08/2024                     |   |
| stevehoover/warp-v            | 223            |       | BSD-3-Clause | 19                       | 15/09/2024                     | CPU Generato                              |
| openhwgroup/core-v-mcu        | 164            |       |              | 1                        | 18/01/2024                     |   |
| rafaelcalcada/steel-core      | 146            |       | MIT          | >30                      |                                |   |
| tommythorn/yarvi              | 82             |       | ISC          | 10                       |                                |   |
| klessydra/T13x                | 43             |       |              | 1                        | 24/08/2024                     |   |
| hgeisse/eco32                 | 35             |       | BSD-2-Clause | 9                        |                                |   |
| munetomo-maruyama/mmRISC-1    | 34             |       | BSD-2-Clause | 6                        | 01/09/2024                     |   |
| whutddk/Rift2Core             | 32             |       | Apache-2.0   | >30                      |                                |   |

64-bit CPUs

32-bit CPUs

Unsuitable designs

Exotic designs

### GR765 - Rad-hard Microprocessor in ST 28nm FDSOI



- Octacore LEON5 SPARC or NOEL-V RISC-V in 28nm SOI
- Dual-Issue in-order 7-stage pipeline, Harvard, RV64GCH – 64-bit
- 64 Base integer instructions (I); MUL/DIV (M); Atomics; Half/Single/Double Precision Float (Zfhmin, FD); Compressed instructions (C); Hypervisor (H); Bit manipulation (subset of) (B); Physical Memory Protection (PMP); MMU - 39 bit virtual addressing, separate I and D, fully associative, TLB
- Cache control extensions: Cacheline invalidate, zero, etc (Zicbom, Zicbop, Zicboz); Cachability in page tables (Svpbmt)
- RISC-V Advanced Interrupt Architecture (AIA)
- Improved interconnect

#### Performance:

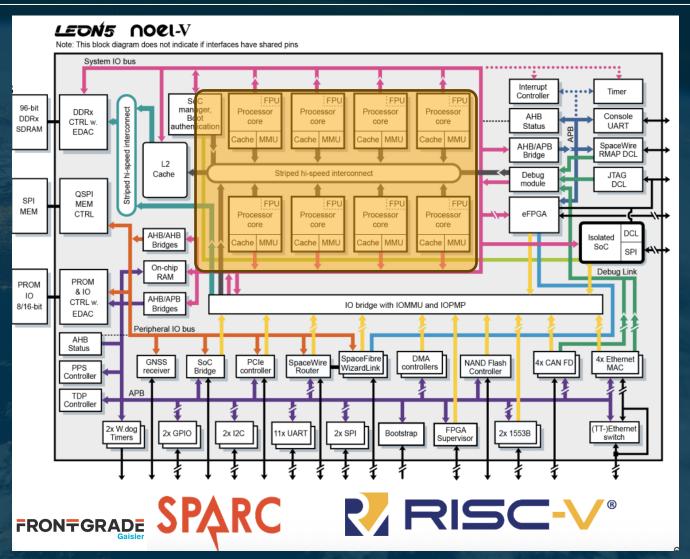
- Comparable to ARM Cortex A53
- CoreMark\*/MHz: 5.02\*\*

goc (ge0886d8ad) 15.0.1 20250330 (experimental)

-0.3-ffast-main-march=n64Imafdc 2ab\_zb\_ 2bc\_zbs\_zbkc\_zbkc\_zbkc\_zbkx\_zicond\_zifencei\_zfl\_zicbom -mabi≡lp64dfinline-functions –param max-inline-insns-auto=20 --param inline-min-speedup=10 -funswitch-loops -funroll-all-loops
fgcse-after-reload -fpredictive-commoning -fipa--cp-done -falign-jumps=8 -falign-functions=8 --param=11-cache-linesize=32 - param=11-cache-size=16

\*\* Using "#define ee\_u32 int32\_t" in core\_portme.h, as is common for 64 bit RISC

**Tape-out Planned Q4/2025 Prototypes Q2/2026** 



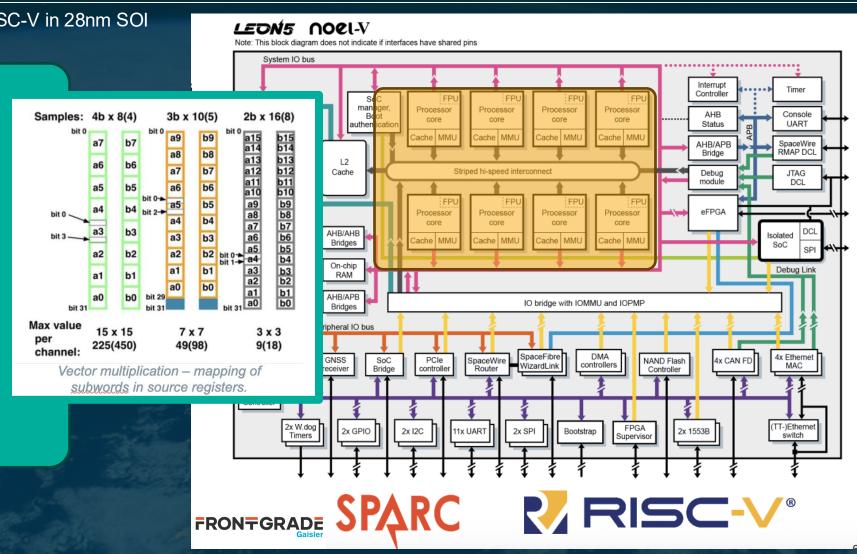
Text and Images from FrontGrade Gaisler, presented at RISC-V in Space 2025.

### GR765 - Rad-hard Microprocessor in ST 28nm FDSOI



- Octacore LEON5 SPARC or NOEL-V RISC-V in 28nm SOI
- SIMD extension (SWAR, daiteq s.r.o.)
- SIMD within a register (SWAR) extensions enable the use of packed instructions.
- Computation of a single instruction on multiple lowresolution operands without penalties.
- Targeted applications:
  - GNSS: 16x2b words;10x3b words; 8x4b words
  - Audio: 2x16b words \
  - Video/image: 4x8b words
- New support: data compression;
   Al

**Tape-out Planned Q4/2025 Prototypes Q2/2026** 



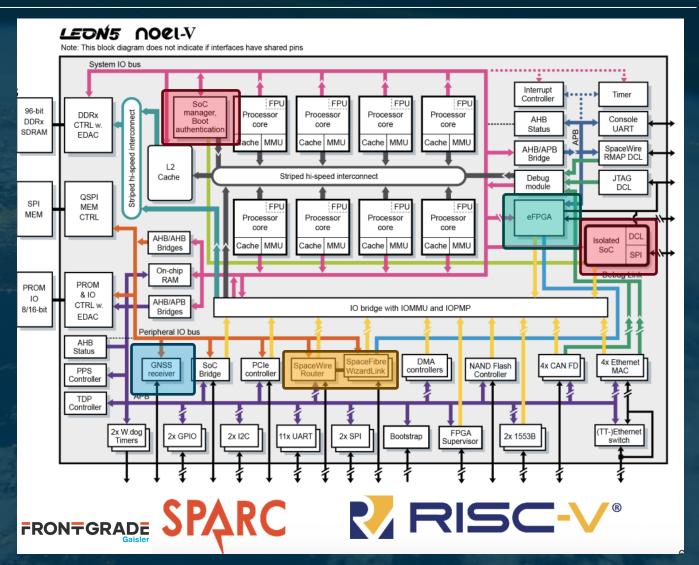
### GR765 - Rad-hard Microprocessor in ST 28nm FDSOI



- Octacore LEON5 SPARC or NOEL-V RISC-V in 28nm SOI
- SIMD extension (SWAR)
- L1 64 KiB/core, striped 4MiB L2 cache
- DDR2/3/4 Memory interface (PHY Nanoxplore)
- QSPI and NAND Flash Controller
- eFPGA 30k LUT (Nanoxplore)
- NavRix GNSS Receiver IP (GPS/GAL, Beyond Gravity AT)
- PQC authenticated boot (Xiphera FI)
- Isolated SoC for authentication / crypto / RoT
- SerDes MIPHY (ST Microelectronics) 6.25 Gbit/s
- 8 lanes PCle Gen3 (Synopsys controller)
- 4 lanes SpFi, bridge to SPW router, WizardLink
- Ethernet switch and TTEthernet (TTTech AT)
- SOC Bridge, FPGA supervisor, CAN-FD
- Package FF1924 no LVDS IO's

**Tape-out Planned Q4/2025** 

**Prototypes Q2/2026** 



Text and Images from FrontGrade Gaisler, presented at RISC-V in Space 2025.

### **Ultra Deep Submicron (UDSM)**



- Development in the scope of the EEE Space Component Sovereignty for Europe.
- Collaborative approach among: ESA & EC & EDA & CNES

Text and Images from Boris Glass (<u>boris.glass@esa.int</u>), ESA presented at RISC-V in Space 2025.

UDSM 0 started

UDSM assessment for onboard digital processors

**ARTES AT 5C.443 – 2M** 

# Main Objective: Next Gen GPP

- Develop next generation
   European space General
   Purpose Processor, based
   on open-source RISC-V and exploiting N7 FinFET
- Develop a mature SW tool ecosystem to exploit multicore parallel processing

UDSM 1 started
UDSM Foundation and platform
technology
GSTP EEE GT3-101ED -19 ME

UDSM 2 ITT preparation

UDSM interface and System in Package technology

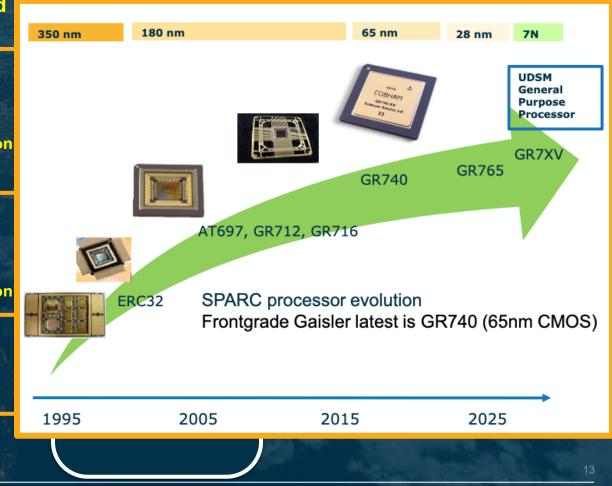
GSTP EEE GT3-102ED -20 ME

UDSM HSSL ITT preparation

GSTP EEE GT3-103ED -2 ME

**UDSM RF IP** 

Converters for telecom beamforming foreseen



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- Development in the scope of the EEE Space Component Sovereignty for Europe.
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### UDSM 0 started

UDSM assessment for onboard digital processors

ARTES AT 5C.443 - 2M

# **General Purpose Accelerator** (GPA)

Develop high performance
European space general
purpose accelerator, based on
open-source RISC-V and
exploiting N7 FinFET.
Applications: Digital Signal
Processing for SAR, Digital
Beamforming, AI.

### UDSM 1 started

UDSM Foundation and platform technology

GSTP EEE GT3-101ED -19 ME

#### UDSM 2 ITT preparation

UDSM interface and System in Package technology

GSTP EEE GT3-102ED -20 ME

UDSM HSSL ITT preparation

GSTP EEE GT3-103ED -2 ME

#### **UDSM RF IP**

Converters for telecom beamforming foreseen

European supply chain for UDSM ICs

Rad-Hard design libraries

**IP Cores** 

Technologies FDSOI 22nm FinFET 7nm

#### UDSM 3 GPP

UDSM General Purpose Processor SoC including eFPGA

foreseen

#### **UDSM FPGA**

SoC including processor cores

foreseen

UDSM RF
Beamforming SoC
foreseen

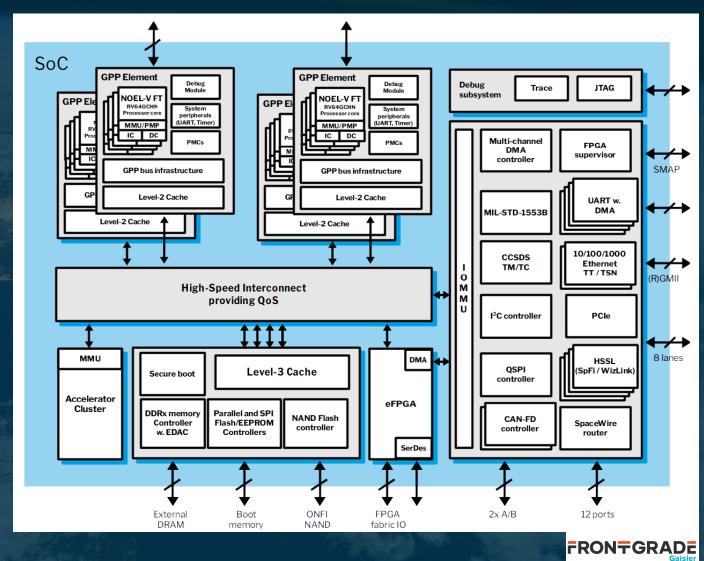
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### **GR7xV - Move to "HPC" in space**



# Rad-hard Microprocessor in 7nm TSMC FinFET

- On hold; priority for GR765
- Clock frequency not much higher than GR765
- 16 cores (4x4 = 4 clusters a 4 cores each)
- 1 RISC-V Vector (RVV) unit per cluster
- VPU to be selected (BSC, ARA...)
- NoC to be selected (Chalmers, Arteris...)
  - AMBA CHI Cache coherency
- Accelerator evaluation : monolithic or SIP
- eFPGA: monolithic eFPGA or SIP
- SerDes, die-to-die (D2D), DDR4+
- Schedule tightly linked to EEE initiative (UDSM)
  - UDSM1 downscaled prototypes ~2027
  - UDSM3 full-size silicon ~2028
  - FM ~2030



### RISC-V in Space HW and SW ecosystem



Activities aiming at supporting the use of RISC-V space micro processors.

IP Core validation/maturation & extensions

Verification and compliance tests using open source and commercial test suited and developing new testcases.

Integration of a Vector Processing Unit.

Development of a microcontroller IP soft core for space FPGA targets.

Space specific extensions of Software Ecosystem.

Specific optimization of GCC compiler.

Driver development for RTEMS and Linux.

Container solutions.

Instruction Set Simulator (ISS) and Software development tools.

NOEL-V simulator (TSIM)

Debug tool support (Lauterbach, IAR, Ashling) Reference flight board design

Advaced Data Handling Architecture reference flight board design

DDR memory interface optimization.

High speed interconnect with companion FPGA.



Rad-hard demonstrator with LEON5FT SPARC V8 32-bit processor and NOEL-V RISC-V 64-bit processor ST 28nm FDSOI GEO P2 technology



GR765 FPGA prototype on development board GR-CPCIS-XCKU115











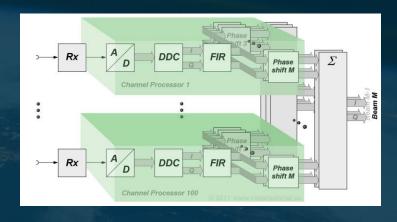




### Space applications needs



- Space-specific benchmarks → architecture selection and configuration → design and space exploration -> OBPMark (<a href="https://github.com/OBPMark">https://github.com/OBPMark</a>)
- Application Development Environment (SDE) → ease of use, qualifiable, open
   ML framework
- HW-SW co-design, design space exploration.
- Security: PQC Encryption, root of trust, authenticated boot
- Performance: more demanding algorithms being used on-board
  - Higher resolution image processing/compression.
  - Software defined radio, beamforming, DVB-S, 5G-NTN
  - AI/ML -> satellite autonomy, FDIR
  - Filters, correlations, CNN with extensive use of parallel/vector operations.
  - Non-linear functions.
  - Data type support for quantized computation (INT16, 8, 4) BFLOAT 16
- Fault Tolerance -> COTS characterisation, space standard qualification.
- Low power/manageable power.



Digital beamforming



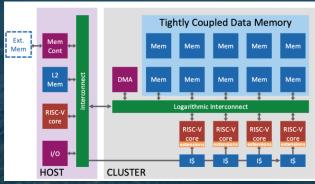
The Copernicus
Hyperspectral Imaging
Mission for the Environment,
CHIME, will carry a unique
visible to shortwave infrared
spectrometer to provide
routine hyperspectral
observations to support new
and enhanced services for
sustainable agricultural and
biodiversity management, as
well as soil property
characterisation

### **Future architectures**

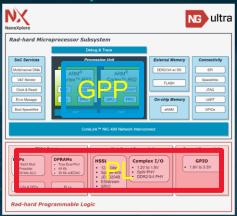


- ESA cannot impose roadmaps -> advisory role.
   Member states and industry supportis needed. Make a useful product with people, IP and fabs available in ESA Member States.
- Architecture selection
  - Ahead of user's needs/feedback.
  - Area/Energy efficiency
  - Flexibility for multiple application domains.
  - Feasibility, affordability.
  - Add parallel, vector & matrix processing →
     3 pillars : GPP, PL/FPGA, VPU/NPU
- Solutions
  - All-in-one devices e.g. AMD(Xilinx) Versal
  - Domain specific accelerators.
  - Out-of-order execution.
  - Many-core processor

### ETHZ - PULP



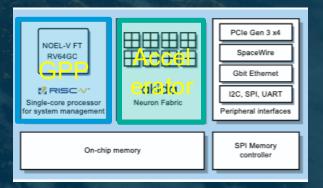
#### NanoXplore NG-Ultra



#### AMD Versal



# FGG – Brainchip akida accelerator



### RISC-V is taking has taken over



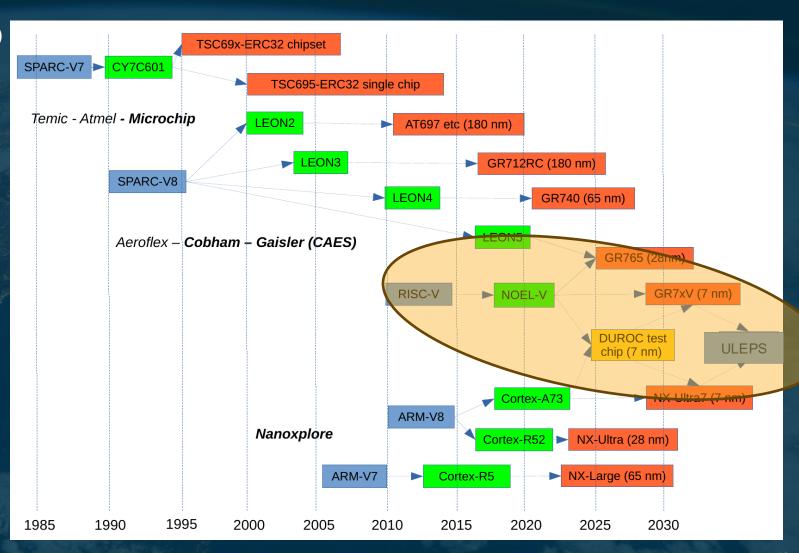
- Today (65/28nm)
- Frontgrade Gaisler (FGG) and Nanoxplore (NX)
  use same chip technology, but different ISA
  SPARC, ARM and RISC-V
- NASA has invested 50 M\$ in RISC-V
- Microchip HPSC
- NX/FGG: cooperation on DUROC RISC-V test chip in 7nm
- 2030 (7nm)

NG-Ultra7: large FPGA with CPU ISA ARM or RISC-V ISA (TBD) GR7xV: large RISC-V, eFPGA

 towards ULEPS UniVersal LowPower European Processor for Space

(RH alternative to AMD Versal...?)

- RISC-V ISA multi-core CPU
- Large FPGA fabrics
- Accelerator (COTS / RH)
- Monolithic or chiplets in SIP



### Conclusions





RISC-V technology is increasingly being adopted in space missions.



Space-specific technical constraints require extensive testing and system-level mitigation to ensure long-term reliability.



Open ISA like RISC-V offer flexibility, non-dependence, and customization.



Development update of GR765 rad-hard microprocessor in ST 28nm FDSOI technology and GR7xV in 7nm TSMC FinFET.



Collaboration between ESA, EC, EDA, and CNES enable the development of RISC-V processors in the frame of UDSM.



Future architectures for space systems will benefit from parallel, vector, and matrix processing capabilities.



Continued investment and cooperation in RISC-V will drive progress in space applications and processor development.









