



# The Significance of the RVA23 Profile in Advancing the RISC-V Ecosystem

Mark Hayter, CSO and Co-Founder, Rivos Inc.

# Open ISA

## Software Ecosystem

(OSes, Platforms, Libraries,  
Domain specific applications)



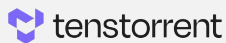
## ISA: Instruction Set Architecture

(Interface between  
Hardware & Software)



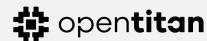
## Implementation: IP

May leverage open and/or  
proprietary IP

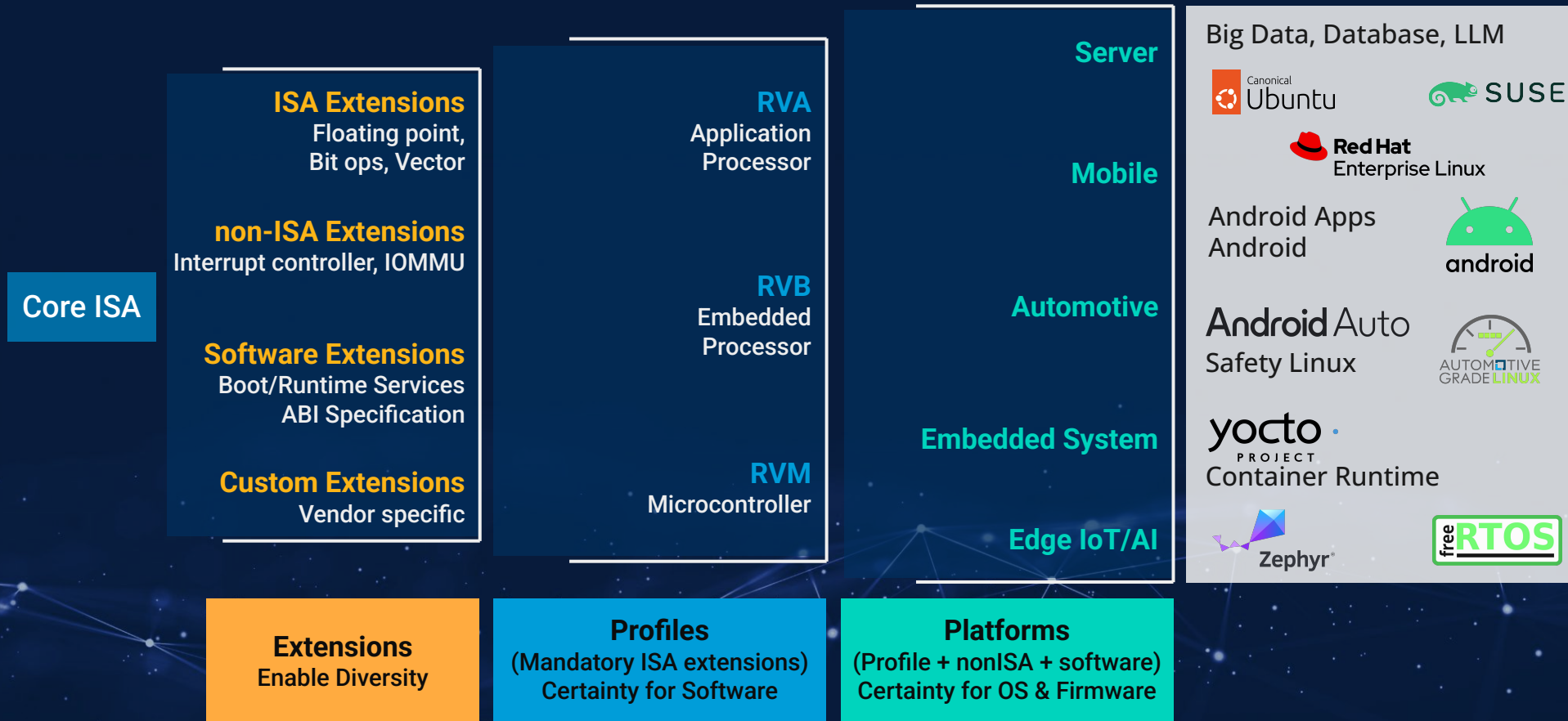


## Implementation: SoC

Competitive opportunity



# Profiles, Platforms and the Software Ecosystem



# Importance of Profiles

- Standard ISAs are critical to the growth of both hardware and software ecosystems
- RISC-V gains broad applicability from many extensions and vendor extensions
- Promote compatibility, innovation and make adoption easier
- Profiles cover different domains: Application (RVA), Embedded (RVB) & Microcontroller



**Mobile**



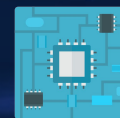
**Laptops**



**Servers**



**Embedded**



**Microcontrollers**

## RVA23 Profile

- Certainty for developers writing applications: binary distribution, download from repo/store
- Standardizes the 64-bit application processors ISA
- Enables seamless user level (application) software portability across hardware implementations

**Enables RISC-V software ecosystem to flourish across industries and application spaces**

# Importance of Platforms

- Operating systems and distributions have more than just the application software
- Promote compatibility, innovation and make adoption easier
- Platforms cover different domains: Server, Mobile, Automotive,...



**Mobile**



**Laptops**



**Servers**



**Auto**

## RISC-V Server Platform (upcoming)

- Certainty for OS developers and full distribution suppliers
- Builds on RVA23 Profile, Server SOC Spec, Boot & Runtime Services Spec, and Security Model
- Enables OS and hypervisor vendors to support multiple RISC-V vendors with a single binary OS image

**Platform Specifications align RISC-V to industry standards; enabling solutions from all vendors to work**

# Benefits from RVA23 for Auto and Server



## Auto

Auto needs structure, consistency and coordination

- Instructions that software can rely on to be present
- Consistent hardware implementations across a range of RISC-V suppliers
- Automotive SIG defining strategy for value chain coordination
- Scalable profiles covering ECU, Zonal Controllers and Central car compute areas



## Server

Teams deploying servers need confidence things will work; RVA23 and RISC-V Server specification together enable this.

- OS and hypervisor vendors support different SoCs with a single binary OS image
- App vendors provide a single binary image
- Security from pre-boot to application
- RAS and Management



# Benefits from RVA23 for Mobile and Laptops



## Mobile

Energy-efficient performance and downloadable Apps from a Store. RVA23 enables this.

- Vector extensions enable AI, media, string/memory... at required speeds
- Significant code density improvements with Bit manipulation and other "ambient" instructions
- Binary compatibility allows single Apps across vendors
- Enables consistent, performant implementations
- Basis for OS platform spec



## Laptops

Client devices need installable application packages and running multi-user and protected environments. RVA23 enables this.

- Hypervisor extension for additional protection
- Similar requirements to mobile devices
- Enables consistent developer experience for writing for RISC-V, on RISC-V

# Key New User Mode Features in RVA23

## New Mandatory

- V Vector extension (optional in RVA22)
- Zvfmin Vector half-precision floating-point
- Zvbb Vector basic bit-manipulation instructions
- Zvkt Vector data-independent execution latency
- Zihintntl Non-temporal locality hints
- Zicond Integer conditional operations
- Zimop may-be-operations
- Zcmop Compressed may-be-operations
- Zcb Additional compressed instructions
- Zfa Additional floating-Point instructions
- *Zawrs Wait-on-reservation-set instructions*
- Supm Pointer masking, (PMLen=0..7)

## Localized

- Zvkng Vector crypto NIST algorithms with GCM
- Zvksg Vector crypto ShangMi algorithms with GCM

## Development (expected mandatory soon)

- Zabha Byte and halfword atomic memory ops
- Zacas Compare-and-Swap instructions
- Ziccamoc Main memory regions CAS support
- Zvbc Vector carryless multiplication
- Zama16b Misaligned loads, stores, and AMOs

## Optional

- Zfh Scalar half-precision floating-point
- Zbc Scalar carryless multiply
- Zicfilp Landing Pads
- *Zicfiss Shadow Stack*
- Zvfh Vector half-precision floating-point
- Zfbfmin Scalar BF16 converts
- Zvfbfmin Vector BF16 converts
- Zvfbfwma Vector BF16 widening mul-add

Implementations are strongly recommended to raise illegal-instruction exceptions on attempts to execute unimplemented opcodes.



# Key RVA23 new features

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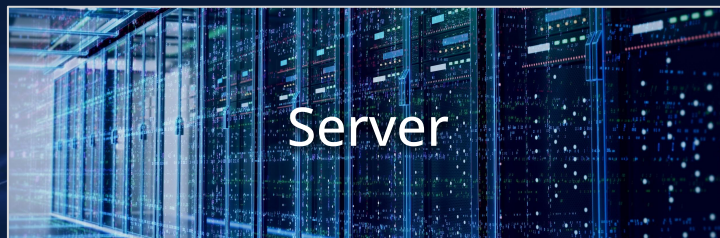
Implementations are strongly recommended to raise illegal-instruction exceptions on attempts to execute unimplemented opcodes.

```
function_entry:
    addi sp,sp,-8
    sd x1,(sp)
    sspush x1
    :
    ld x1,(sp)
    addi sp,sp,8
    sspopchk x1
    ret
```

# Call to Action: Develop with RVA23

**RISC-V CPU developers:** make your processor available for binary application distribution

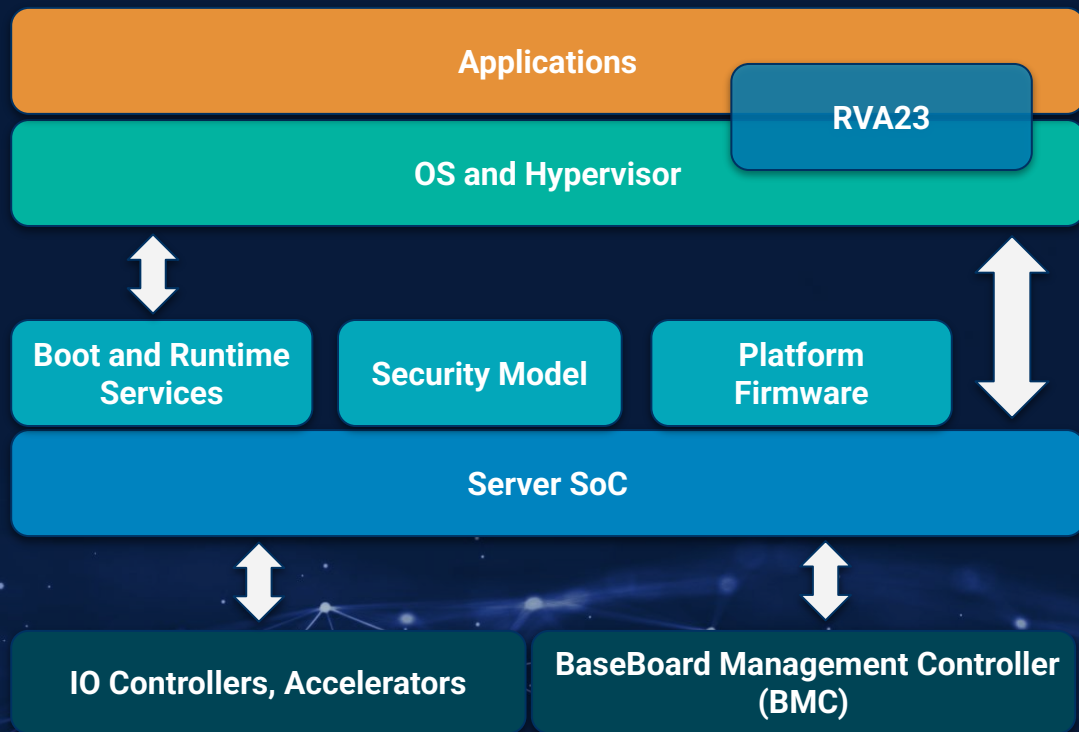
**RISC-V Application developers:** use RVA23 as your optimization target



Compatibility and efficiency for industries reliant in virtualized, scalable and secure capabilities

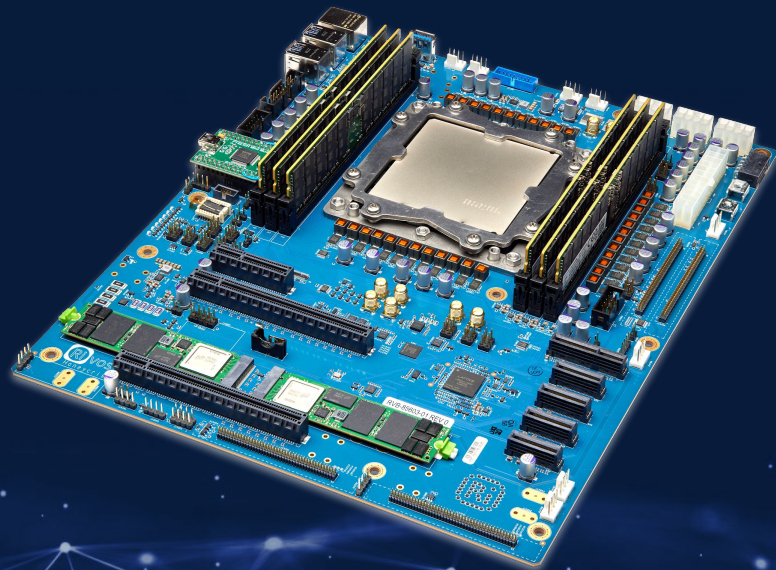
# RISC-V Server Platform: Built on RVA23

- Standardized SoC hardware interfaces such as PCIe root ports, IOMMU, and Interrupt Controllers
- Boot and Runtime services using UEFI and ACPI
- BMC for provisioning and management using standards such as MCTP, PLDM, IPMI, and Redfish
- Security Model guides debug authorization, secure boot, firmware updates, firmware resilience, and other use cases



# RISC-V Server SoC Specification Outline

- Clocks, Timers, and Interrupt Controllers
- IOMMU
- PCIe Subsystem
  - ECAM and PCIe memory space
  - Access Control Services
  - Handling of ID and address routed transactions
  - Message Signaled Interrupts
  - Precision Time Management
- Reliability, Availability, and Serviceability
- Quality of Service
- Manageability
- Performance Monitoring
- Security



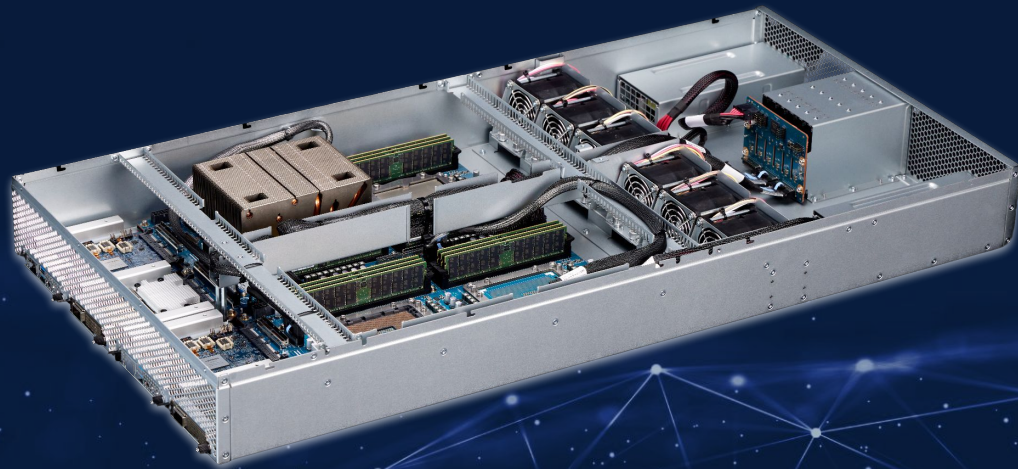
**Enables OS and hypervisor vendors to support SoCs with a single binary OS image distribution model**



# Call to Action: Help Final Stages of Server Platform

**Specification is going to Public Review: please help with feedback**

**Server SoC developers: Adopt the Platform Specification for your parts**



**Compatibility and efficiency for industries reliant in virtualized, scalable and secure capabilities**

# Building the Server Software Ecosystem Together

“

Hardware and software vendors are rallying around the RVA23 profile to bring consistency to the enterprise and high-performance compute landscape.

Through close collaboration, Rivos and Canonical are enabling the benefits of standardization on RISC-V whilst opening up the flexibility for vendor-specific optimizations. This balanced approach ensures stability, security, and performance. These requirements are essential for robust and performant enterprise solutions.

– Gordan Markus Director, Silicon Alliance, Canonical

”

Rivos and Canonical bring RISC-V Ubuntu for Data Centers

Enabled by RVA23 Profile and Server Platform

**Same** distribution will work for all vendors following the specs



<https://www.youtube.com/@RivosInc/videos>



# Shameless Plug for RISC-V Taipei Day & Computex

ASpeed will show the Rivos DC-SCM card with their  
AST2750 BMC at their Computex booth

**2025 RISC-V  
Taipei Day**

## **Pioneering AI with RISC-V**

**Built on Open Standards, Secure for Tomorrow**

**May 20-23** **PAVILION**

Booth L0425 4F, TaiNEX 1, Taipei

**May 21** **CONFERENCE**

Room 505 5F, TaiNEX 1, Taipei

Organizer:



台灣物聯網產業技術協會  
Taiwan IoT Industry Technology Association

Co-Organizer:



Intendend to open the KiCAD schematics  
(and web viewable schematic)

# Shared Vision based on Standards



**Building a stronger RISC-V ecosystem together with Profiles and Platforms**