Implementation of Branch Treatment Strategies in the **Ripes** RISC-V Simulator

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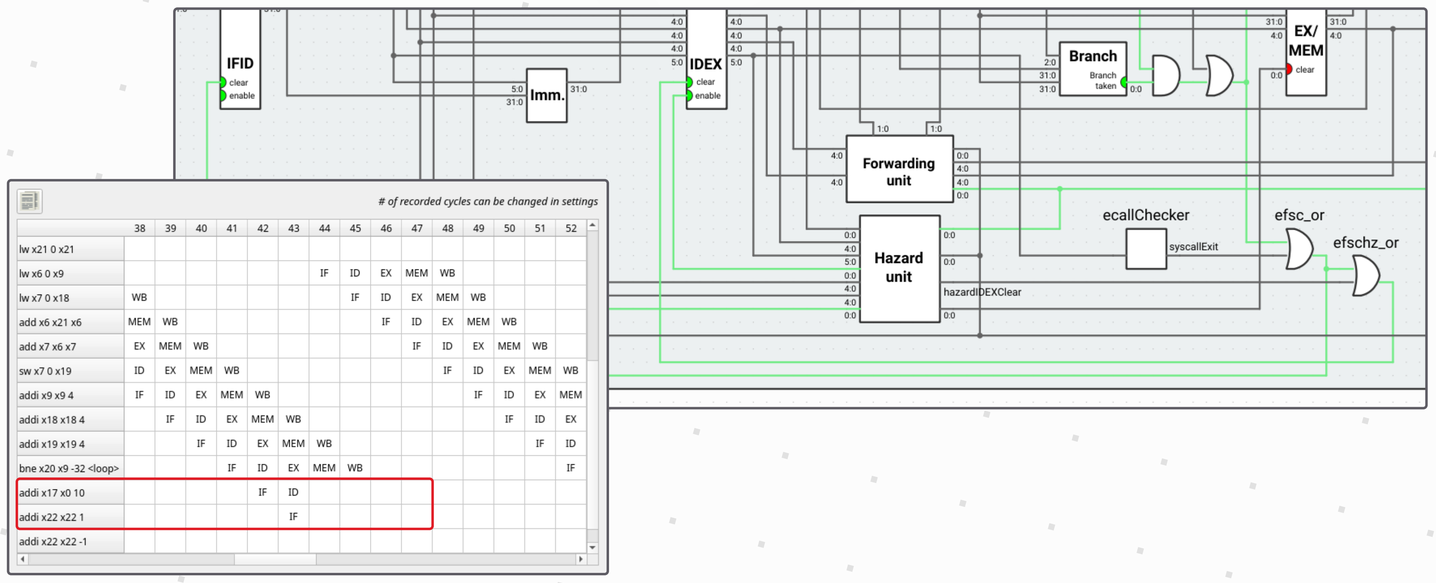
Before

Ripes currently only has one branch strategy for its pipelined processors: predict-not-taken, resolved in the EX stage for two* delay slots.

This was insufficient for our Computer Organisation course curriculum, where we want to explore the impact of different strategies on the performance of program execution.

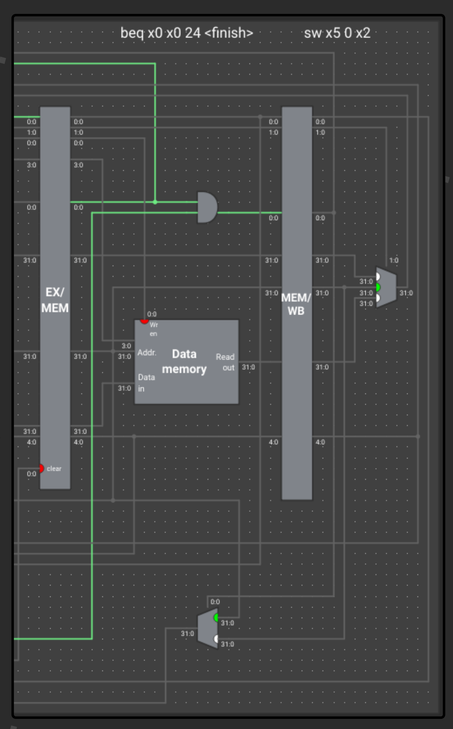
* Three, in the case of the two-way superscalar model.

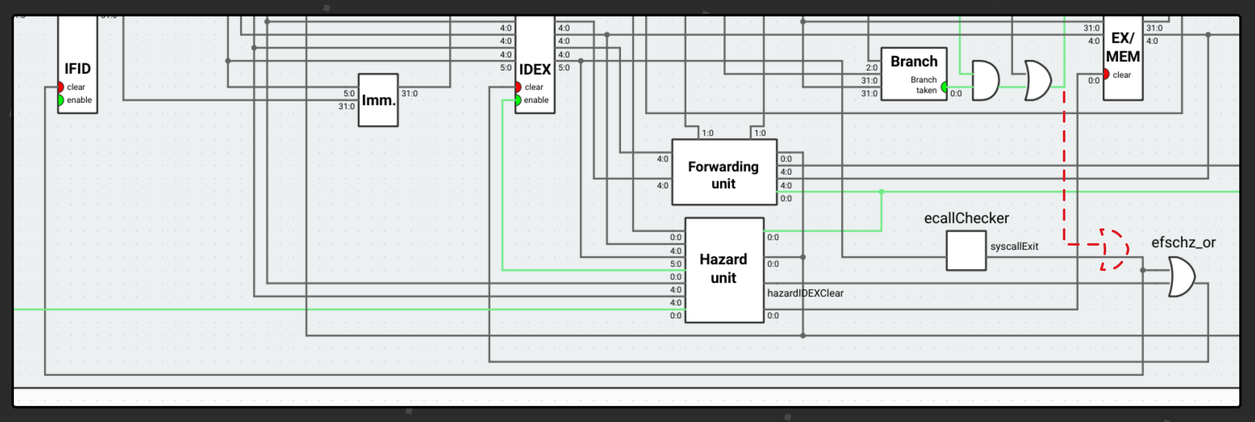


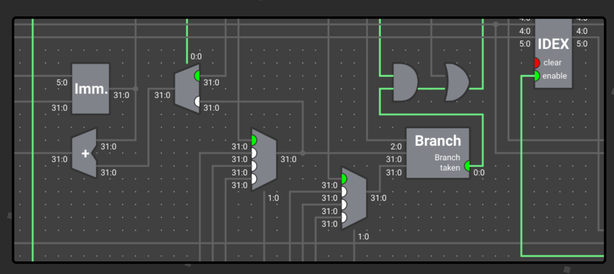
	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52
lw x21 0 x21															
lw x6 0 x9							IF	ID	EX	MEM	WB				
lw x7 0 x18	WB						IF	ID	EX	MEM	WB				
add x6 x21 x6	MEM	WB						IF	ID	EX	MEM	WB			
add x7 x6 x7	EX	MEM	WB						IF	ID	EX	MEM	WB		
sw x7 0 x19	ID	EX	MEM	WB						IF	ID	EX	MEM	WB	
addi x9 x9 4	IF	ID	EX	MEM	WB						IF	ID	EX	MEM	
addi x18 x18 4		IF	ID	EX	MEM	WB						IF	ID	EX	
addi x19 x19 4			IF	ID	EX	MEM	WB						IF	ID	
bne x20 x9 -32 <loop>				IF	ID	EX	MEM	WB							IF
addi x17 x0 10					IF	ID									
addi x22 x22 1						IF									
addi x22 x22 -1															

After

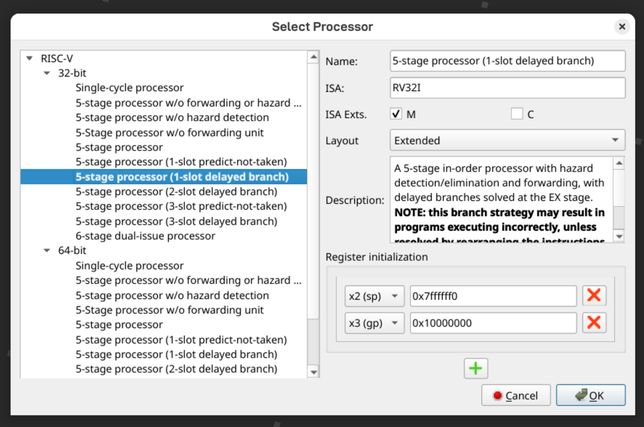
Thanks to Ripes' modular processor models, we were able to implement our additional branch treatment strategies as five additional models. In these models, which we based on the five-stage pipelined processor with hazard detection and forwarding, the circuitry was modified to achieve the desired behaviour.

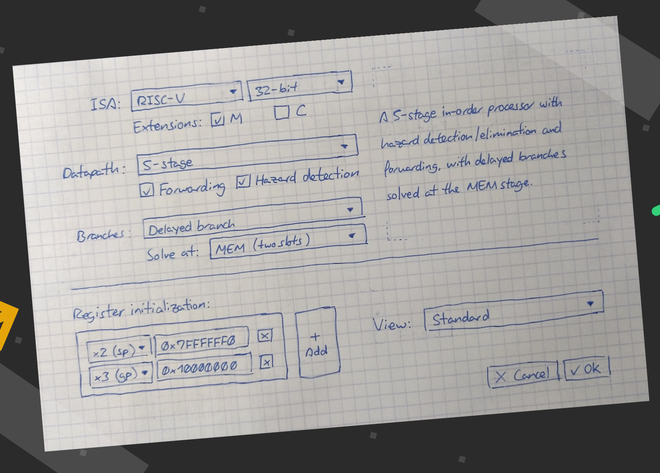


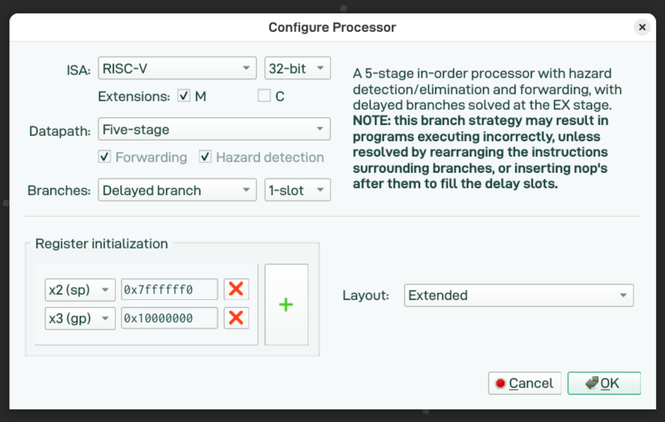




The increased number of models made the existing processor selection dialog awkward to use, so it was redesigned to allow the user to select a processor based on its individual characteristics. To enable this, Ripes' processor registry was leveraged to add the necessary metadata to the processor models.







Results

The five-stage pipelined processor in our Ripes fork can now be set up with one, two, or three delay slots, with both predict-not-taken and delayed branches, with the effect on program execution seen here.

	47	48	49	50	51	52	53	54	55	56	57	58	59	60
lw x21 0 x21														
lw x6 0 x9					IF	ID	EX	MEM	WB					
lw x7 0 x18	WB					IF	ID	EX	MEM	WB				
add x6 x21 x6	MEM	WB					IF	ID	EX	MEM	WB			
add x7 x6 x7	EX	MEM	WB					IF	ID	EX	MEM	WB		
sw x7 0 x19	ID	EX	MEM	WB					IF	ID	EX	MEM	WB	
addi x9 x9 4	IF	ID	EX	MEM	WB					IF	ID	EX	MEM	WB
addi x18 x18 4		IF	ID	EX	MEM	WB					IF	ID	EX	MEM
addi x19 x19 4			IF	ID	EX	MEM	WB					IF	ID	EX
bne x20 x9 -32 <loop>				IF	ID	EX	MEM	WB					IF	ID
addi x17 x0 10					IF									
addi x22 x22 1														

# of recorded cycles can be changed in settings

← Predict not taken

Delayed branches →

	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58
lw x21 0 x21																		
lw x6 0 x9								IF	ID	EX	MEM	WB						
lw x7 0 x18	WB							IF	ID	EX	MEM	WB						
add x6 x21 x6	MEM	WB							IF	ID	EX	MEM	WB					
add x7 x6 x7	EX	MEM	WB							IF	ID	EX	MEM	WB				
sw x7 0 x19	ID	EX	MEM	WB							IF	ID	EX	MEM	WB			
addi x9 x9 4	IF	ID	EX	MEM	WB							IF	ID	EX	MEM	WB		
addi x18 x18 4		IF	ID	EX	MEM	WB							IF	ID	EX	MEM	WB	
addi x19 x19 4			IF	ID	EX	MEM	WB							IF	ID	EX	MEM	
bne x20 x9 -32 <loop>				IF	ID	EX	MEM	WB							IF	ID	EX	
addi x17 x0 10					IF	ID	EX									IF	ID	
addi x22 x22 1						IF	ID										IF	
addi x22 x22 -1							IF											
ecall																		

	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65
lw x21 0 x21																
lw x6 0 x9							IF	ID	EX	MEM	WB					
lw x7 0 x18	WB							IF	ID	EX	MEM	WB				
add x6 x21 x6	MEM	WB							IF	ID	EX	MEM	WB			
add x7 x6 x7	EX	MEM	WB							IF	ID	EX	MEM	WB		
sw x7 0 x19	ID	EX	MEM	WB							IF	ID	EX	MEM	WB	
addi x9 x9 4	IF	ID	EX	MEM	WB							IF	ID	EX	MEM	WB
addi x18 x18 4		IF	ID	EX	MEM	WB							IF	ID	EX	MEM
addi x19 x19 4			IF	ID	EX	MEM	WB							IF	ID	EX
bne x20 x9 -32 <loop>				IF	ID	EX	MEM	WB							IF	ID
addi x17 x0 10					IF	ID	EX	MEM	WB							IF
addi x22 x22 1						IF	ID	EX	MEM	WB						
addi x22 x22 -1							IF	ID	EX	MEM	WB					

	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58
lw x21 0 x21																		
lw x6 0 x9								IF	ID	EX	MEM	WB						
lw x7 0 x18	WB							IF	ID	EX	MEM	WB						
add x6 x21 x6	MEM	WB							IF	ID	EX	MEM	WB					
add x7 x6 x7	EX	MEM	WB							IF	ID	EX	MEM	WB				
sw x7 0 x19	ID	EX	MEM	WB							IF	ID	EX	MEM	WB			
addi x9 x9 4	IF	ID	EX	MEM	WB							IF	ID	EX	MEM	WB		
addi x18 x18 4		IF	ID	EX	MEM	WB							IF	ID	EX	MEM	WB	
addi x19 x19 4			IF	ID	EX	MEM	WB							IF	ID	EX	MEM	
bne x20 x9 -32 <loop>				IF	ID	EX	MEM	WB							IF	ID	EX	
addi x17 x0 10					IF	ID	EX	MEM	WB							IF	ID	
addi x22 x22 1						IF	ID	EX	MEM	WB							IF	
addi x22 x22 -1							IF	ID	EX	MEM	WB							
ecall																		

This project is publicly available on GitHub.

Try it!

Acknowledgements

This work has been funded by the Junta de Comunidades de Castilla-La Mancha, under the project SBPLY/21/180225/000103 and the Spanish Ministry of Science, Innovation and Universities under the projects PID2021-123627OB-C52 and TED2021-130233B-C31. Moreover, this work is also funded by Grant Cátedra PERTE Chip University of Castilla-La Mancha (TSI-069100-2023-0014) funded by the Ministry of Digital Transformation (Cátedras PERTE Chip Programme) through the "European Union NextGenerationEU/PRTR".