Implementation of Branch Treatment Strategies in the Ripes RISC-V Simulator

w x6 0 x9

lw x7 0 x18

add x6 x21



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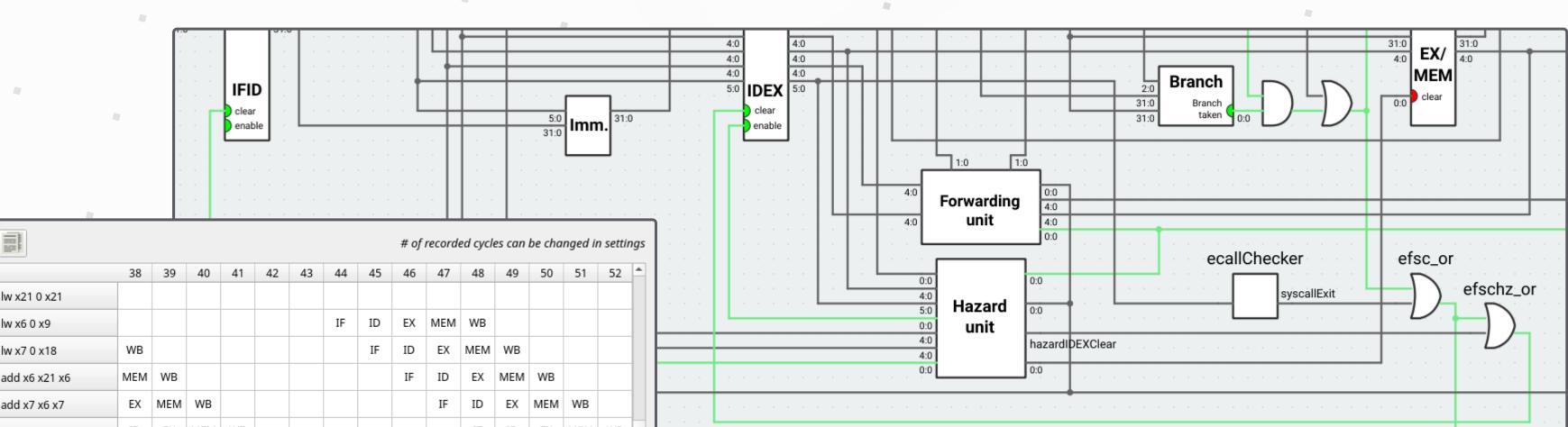
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Before

Ripes currently only has one branch strategy for its pipelined processors: predict-not-taken, resolved in the EX stage for two* delay slots.

This was insufficient for our Computer

Organisation course curriculum, where we want to explore the impact of different strategies on the performance of program execution.

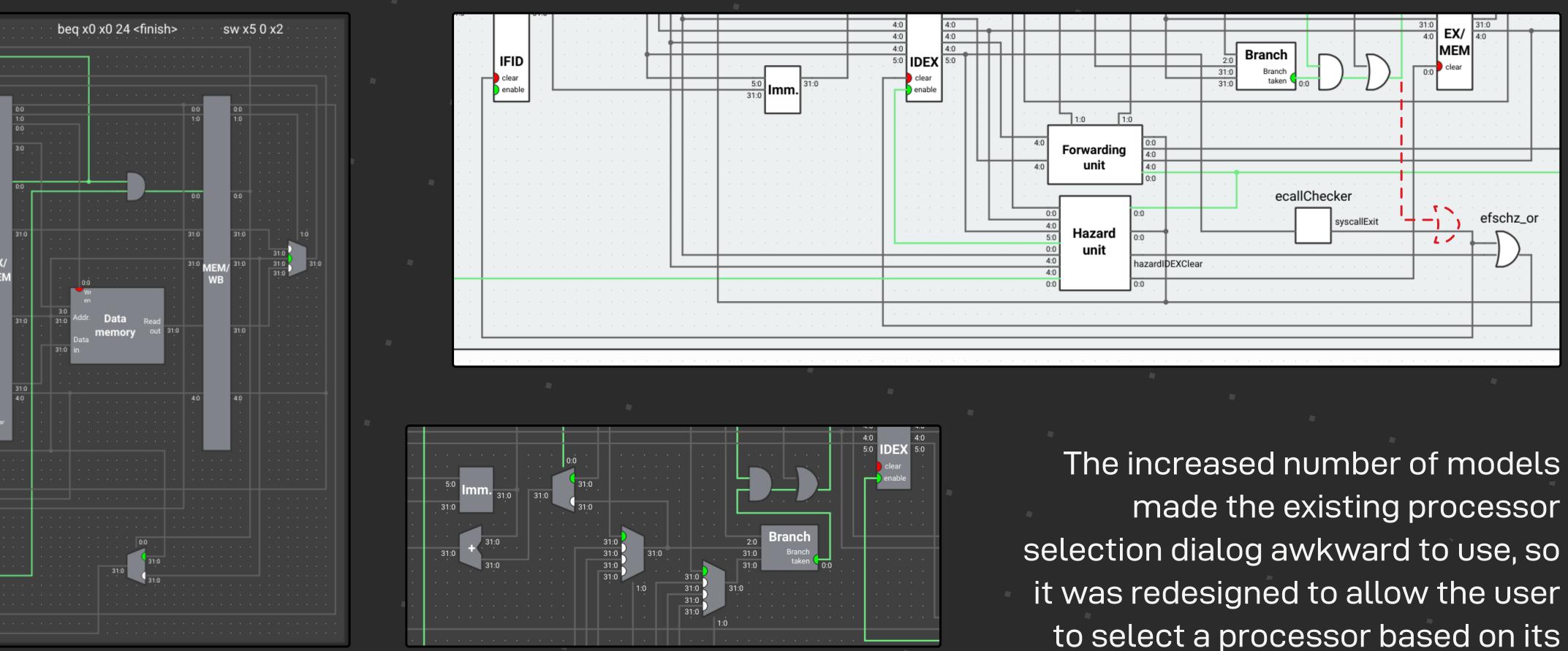


* Three, in the case of the two-way superscalar model.

sw x7 0 x19	ID	EX	MEM	WB							IF	ID	EX	MEM	WB
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After

Thanks to Ripes' modular processor models, we were able to implement our additional branch treatment strategies as five additional models. In these models, which we based on the fivestage pipelined processor with hazard detection and forwarding, the circuitry was modified to achieve the desired behaviour.

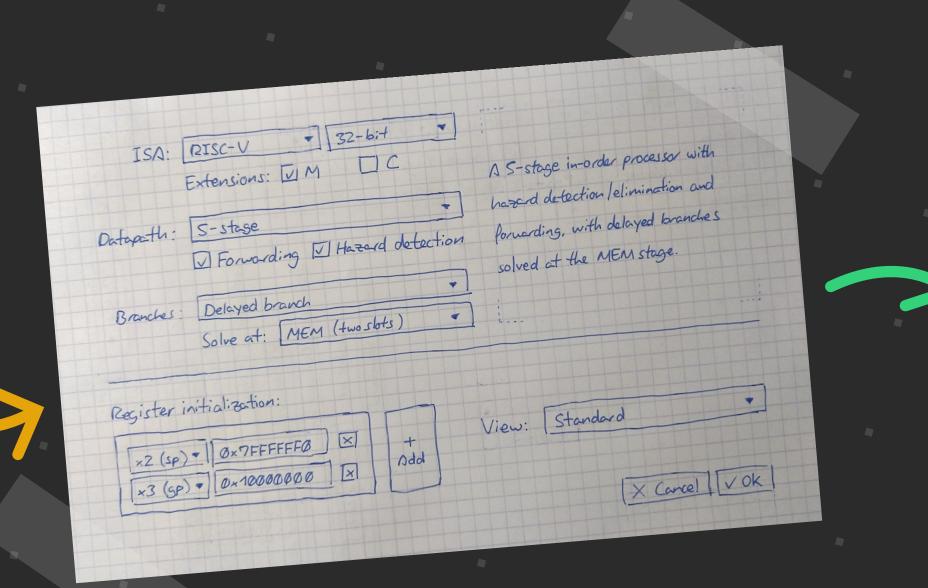


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selection dialog awkward to use, so it was redesigned to allow the user to select a processor based on its individual characteristics. To enable this, Ripes' processor registry was leveraged to add the necessary metadata to the processor models.

	Configu	re Processor	×
ISA:	RISC-V ▼ 32-bit ▼ Extensions: ✓ M □ C	A 5-stage in-order processor with hazard detection/elimination and forwarding, with delayed branches solved at the EX stage.	
Datapath:	Five-stage ✓ Forwarding ✓ Hazard detection	NOTE: this branch strategy may result in programs executing incorrectly, unless resolved by rearranging the instructions surrounding branches, or inserting nop's	
Branches:	Delayed branch 🔹 1-slot	after them to fill the delay slots.	
Register i x2 (sp) x3 (gp)	nitialization	Layout: Extended -	

	Selec	t P	rocessor	
-	RISC-V → 32-bit Single-cycle processor 5-stage processor w/o forwarding or hazard 5-stage processor w/o hazard detection 5-Stage processor w/o forwarding unit			5-stage processor (1-slot delayed brand RV32I M C
	5-stage processor 5-stage processor (1-slot predict-not-taken)		Layout	Extended A 5-stage in-order processor with haza
	5-stage processor (1-slot delayed branch) 5-stage processor (2-slot delayed branch) 5-stage processor (3-slot predict-not-taken) 5-stage processor (3-slot delayed branch) 6-stage dual-issue processor		Description:	detection/elimination and forwarding, delayed branches solved at the EX stag NOTE: this branch strategy may resu programs executing incorrectly, unle
	 64-bit Single-cycle processor 		Register initia	alization
	 5-stage processor w/o forwarding or hazard 5-stage processor w/o hazard detection 5-stage processor w/o forwarding unit 5-stage processor 5-stage processor (1-slot predict-not-taken) 		x2 (sp) x3 (gp)	 0x7fffff0 0x1000000
	5-stage processor (1-slot delayed branch) 5-stage processor (2-slot delayed branch)	Ŧ		+
				• <u>C</u> ancel



-	60	59	58	57	56	55	54	53	52	51	50	49	48	47	
															lw x21 0 x21
					WB	MEM	EX	ID	IF						lw x6 0 x9
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			WB	MEM	EX	ID	IF						WB	MEM	add x6 x21 x6
		WB	MEM	EX	ID	IF						WB	MEM	EX	add x7 x6 x7
	WB	MEM	EX	ID	IF						WB	MEM	EX	ID	sw x7 0 x19
	MEM	EX	ID	IF						WB	MEM	EX	ID	IF	addi x9 x9 4
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										IF					addi x17 x0 10
*															addi x22 x22 1

Results

	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	f
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lw x7 0 x18	WB								IF	ID	EX	MEM	WB						
add x6 x21 x6	MEM	WB								IF	ID	EX	MEM	WB					
add x7 x6 x7	EX	MEM	WB								IF	ID	ΕX	MEM	WB				
sw x7 0 x19	ID	EX	MEM	WB								IF	ID	EX	MEM	WB			
addi x9 x9 4	IF	ID	EX	MEM	WB								IF	ID	EX	MEM	WB		1
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addi x17 x0 10					IF	ID	EX										IF	ID	
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The five-stage pipelined processor in our Ripes fork can now be set up with one, two, or three delay slots, with both predict-nottaken and delayed branches, with the effect on program execution seen here.

← Predict not taken

Delayed branches \rightarrow

•	60	59	58	57	56	55	54	53	52	51	50	49	48	47	
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This project is publicly available on GitHub.

Try it

Acknowledgements

This work has been funded by the Junta de Comunidades de Castilla-La Mancha, under the project SBPLY/21/180225/000103 and the Spanish Ministry of Science, Innovation and Universities under the projects PID2021-1236270B-C52 and TED2021-130233B-C31. Moreover, this work is also funded by Grant Cátedra PERTE Chip University of Castilla-La Mancha (TSI-069100-2023-0014) funded by the Ministry of Digital Transformation (Cátedras PERTE Chip Programme) through the "European Union NextGenerationEU/PRTR"

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add x7 x6 x7	EX	MEM	WB							IF	ID	EX	MEM	WB		
sw x7 0 x19	ID	EX	MEM	WB							IF	ID	EX	MEM	WB	Γ
addi x9 x9 4	IF	ID	EX	MEM	WB							IF	ID	ΕX	MEM	
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bne x20 x9 -32 <loop></loop>				IF	ID	EX	MEM	WB							IF	
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