Snooper: A Flexible Tracing Solution for Fast Simulation and Analysis in RISC-V

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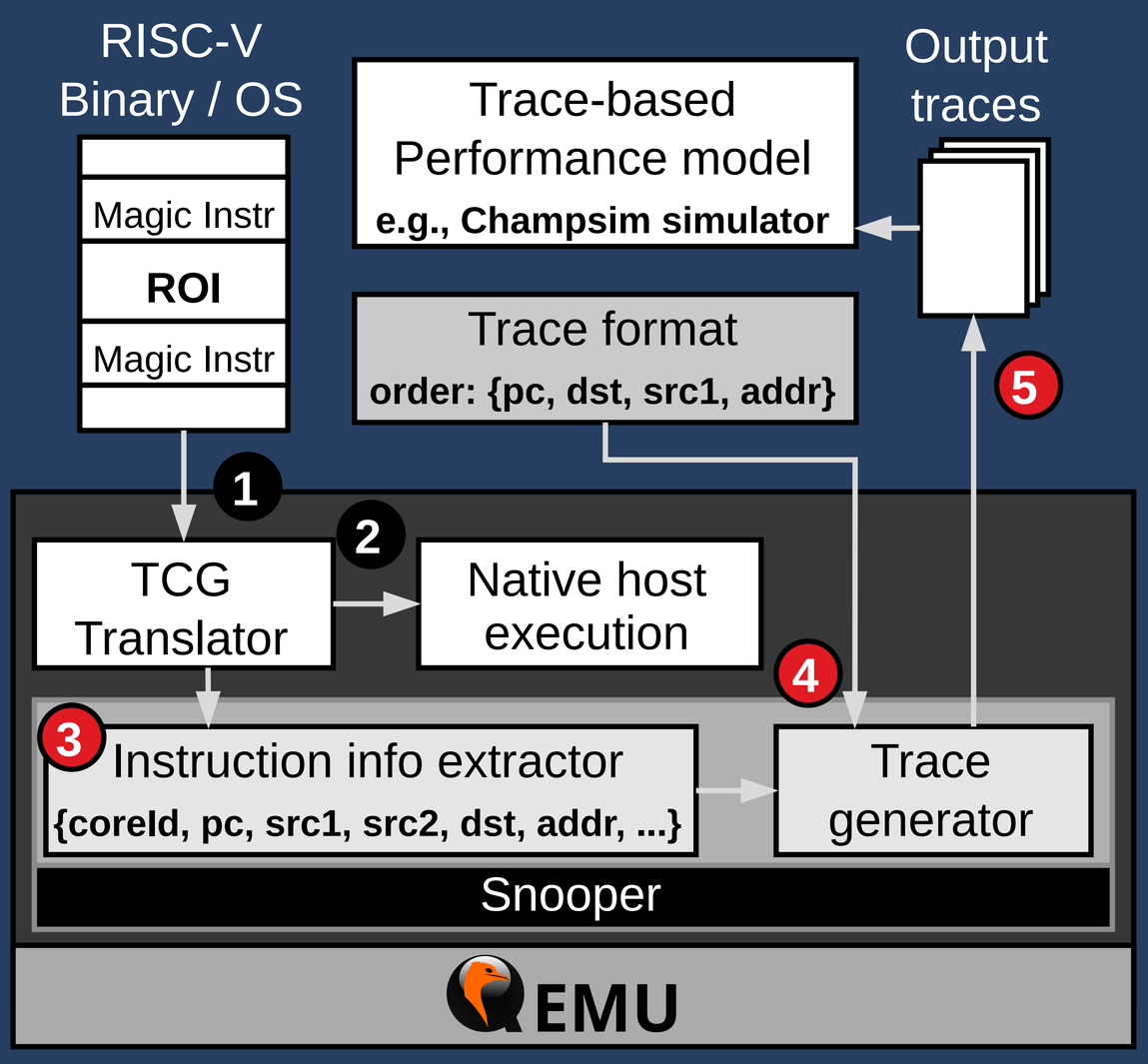
1. Background and motivation

Hardware simulation is essential for computer architecture research.
Trace-based simulators enable fast CPU and memory system modeling.
Existing trace-based simulators lack RISC-V ISA support.
Snooper fills this gap, providing a fast and flexible RISC-V tracing solution.

2. Design and Features

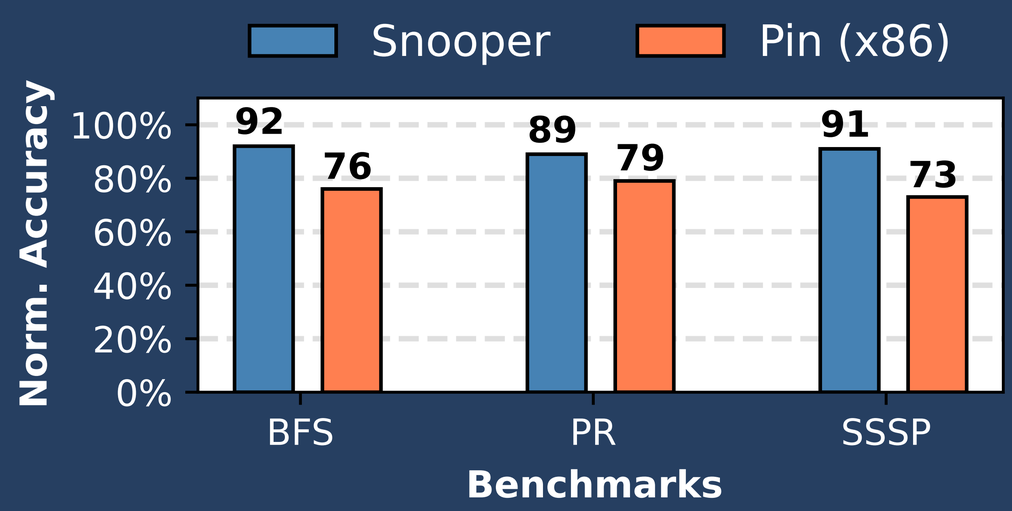
Implemented as a QEMU TCG plugin.
Leverages QEMU's dynamic binary translation.
Extracts metadata characteristics per instruction.
Generates customizable trace files.
Supports user-mode and full-system tracing.
Enables RISC-V OS evaluation.
Two trace generation modes: Plain binary and CSV.



1. QEMU loads executable either a user-mode program or an OS and supports magic instructions to define the Region of Interest (ROI)
2. QEMU translates to IR and executes the code
3. Snooper at the same time as 2 gets the information depending on 4
5. Snooper outputs trace, that then can be analyzed or used in trace-based simulators

3. Evaluation

To validate the accuracy of Snooper's traces, all experimental results are normalized to our in-house RTL SoC execution time (running on an FPGA).
We aim to highlight how existing traces, generated for other ISAs, are unsuitable for evaluating RISC-V performance due to differences in ISA design, compilation tools, and software stack maturity.
We compile the evaluated benchmarks for both RISC-V and x86, generate traces using Snooper and Pin respectively, and evaluate them under the same ChampSim configuration.



Snooper achieves 89% average accuracy.
On average, Pin-based traces perform 2.6 times higher error rates, underscoring the importance of RISC-V trace generation tools for accurate performance evaluation.
Snooper enables fast and accurate RISC-V architecture evaluation.

4. Discussion

Although Snooper generates RISC-V traces, the QEMU TCG plugin shares common data structures across all supported ISAs (e.g., x86 and ARM).
Snooper can be used with simpler analytical models to accelerate simulation time.

References

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