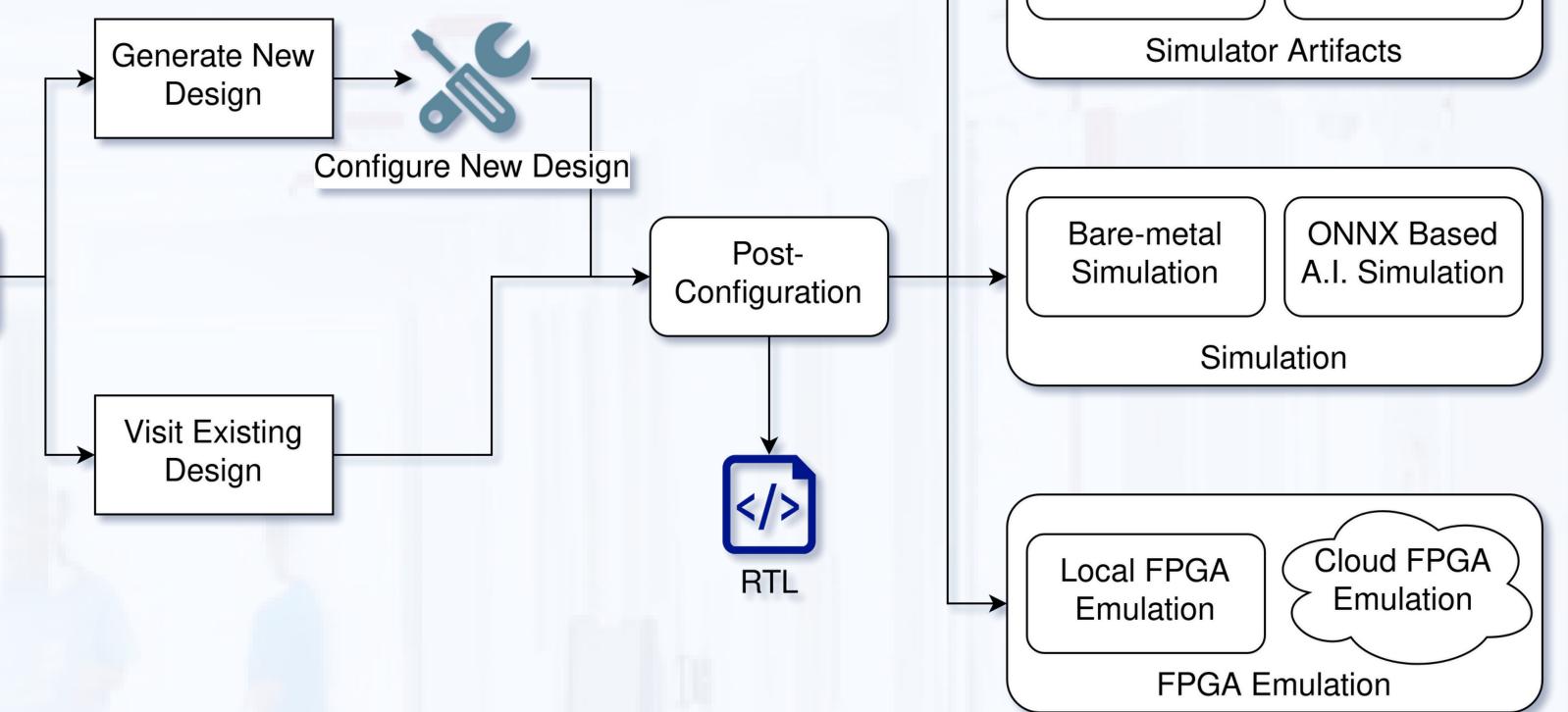
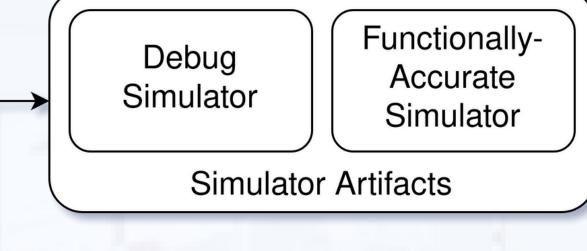


SoC Studio: A User-Centric Framework for **Custom System-on-Chip Design, Emulation,** and AI Integration

Authors: Shayan Hassan Baig, Shahzaib Kashif, Ali Ahmed, Farhan Ahmed Karim

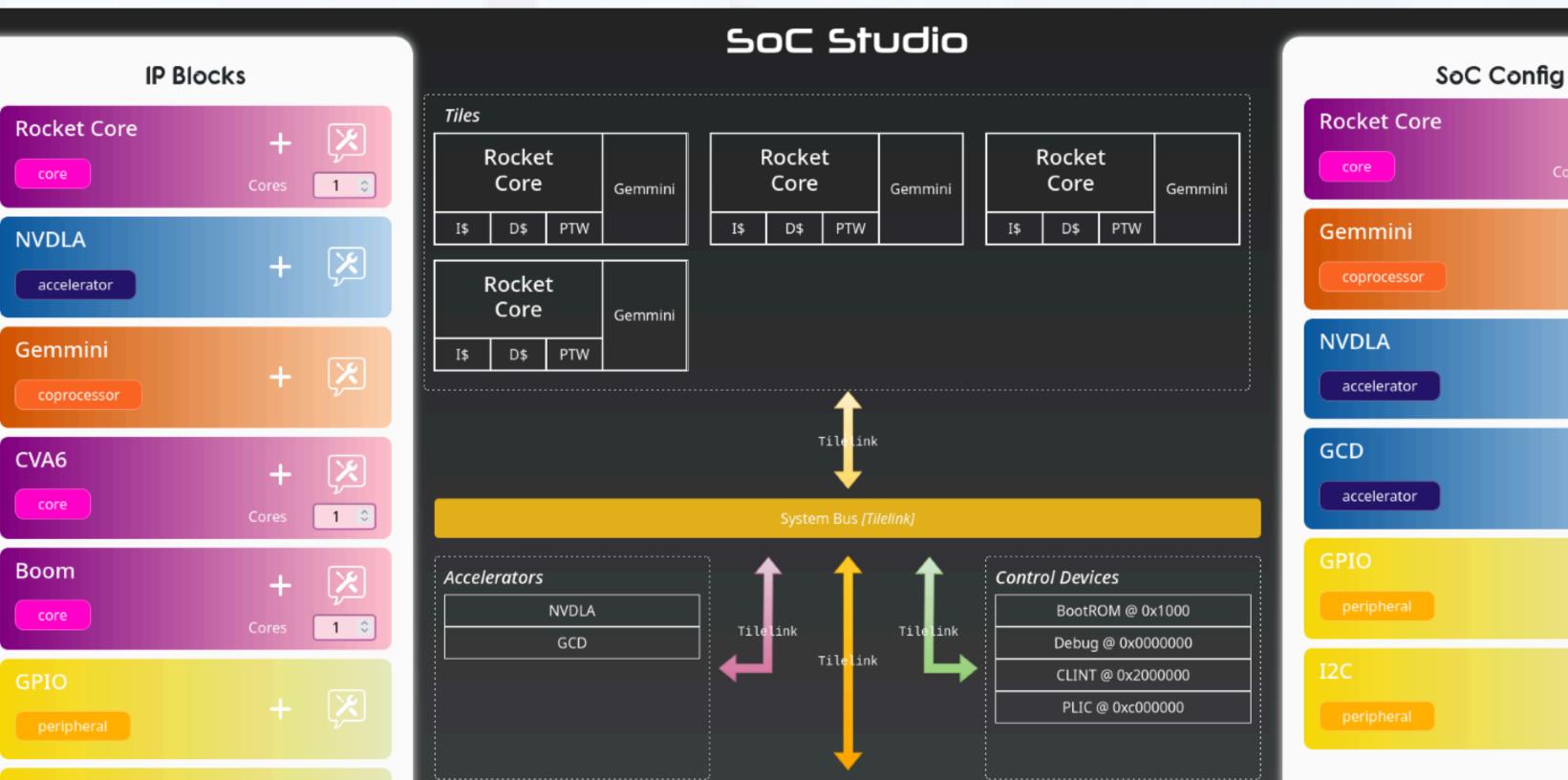
SoC Studio is a web-based application for designing and rapidly prototyping RISC-V designs by enabling users to Dashboard configure, simulate, and emulate custom SoC designs and A.I. inference through an intuitive interface.





FEATURES

GUI Interface



approach helps The GUI users understand and visualize their design while avoiding errors that may arise command line or file-based from approaches

I2C peripheral	+ 🔀	Peripherals UART @ 0x10020000 GPIO	I2C
GCD	+ 🔀		

Artifacts

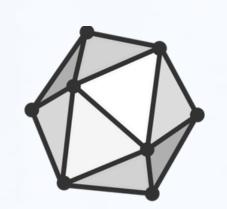


SoC Studio generates RTL of the configured design, a cycle-accurate simulator, called the Debug Simulator, which enables generation of waveforms of baremetal programs and software running on the custom SoC, as well as a functional-accurate simulator which provides only the post-simulation terminal output.

Generate SoC

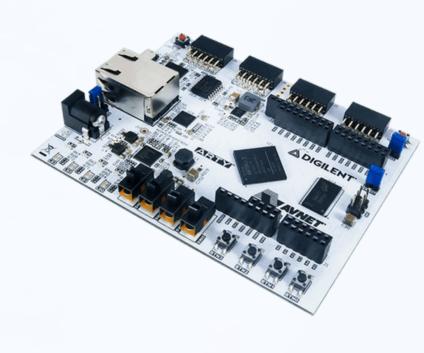
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Simulation



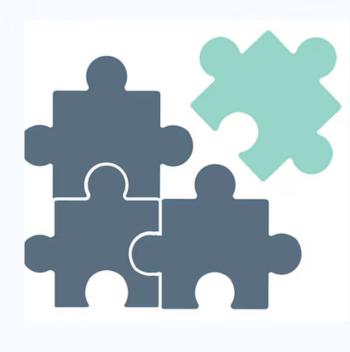
Bare-metal simulation as well as ONNX-based A.I. inferencing simulation, if the design has an A.I. accelerator configured in it. Upload custom or select pretrained ONNX-based A.I. models to run on a RISC-V based ONNX runtime for the simulation.

FPGA Emulation



Deploy designs on cloud-based FPGA instances (e.g., AWS F1) or local boards (e.g. Xilinx Zynq, Intel Altera) for rapid prototyping. Post-emulation, generate comprehensive PPA reports and detailed FPGA resource utilization metrics.

Custom IP Integration



Integrate custom IP blocks into the SoC architecture either by augmenting the Memory-Mapped I/O (MMIO) address space with custom or pre-validated IPs, or attach as a host (core) or a coprocessor. Blackbox abstraction for plug-and-play compatibility of externally developed RTL modules possible via interconnect standards such as Tilelink and AMBA.



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