Croc: An End-to-End Open-Source Extensible RISC-V MCU Platform to Democratize Silicon

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Abstract

Ensuring a continuous and growing influx of skilled chip designers and a smooth path from education to innovation are key goals for several national and international "Chips Acts". Silicon democratization can greatly benefit from end-to-end (from silicon technology to software) free and open-source (OS) platforms. We present Croc, an extensible RISC-V microcontroller platform explicitly targeted at hands-on teaching and innovation. Croc features a streamlined OS synthesis and an end-to-end OS implementation flow, ensuring full, unconstrained access to the design, the design automation tools, and the implementation technology. Croc uses the industry-proven, open-source CVE2 core, implementing the RV32I(EMC) instruction set architecture (ISA), enabling students to define and implement their own ISA extensions. MLEM, a tapeout of Croc in IHP's open 130 nm node completed in eight weeks by a team of just two students, demonstrates the platform's viability for hands-on teaching in schools, universities, or even on a self-education path. In spring 2025, ETH Zurich will utilize Croc for its curricular VLSI class, involving up to 80 students, producing up to 40 OS application-specific integrated circuit layouts, and completing up to five student-led system-on-chip tapeouts. The lecture notes and exercises are already available under a Creative Commons license.

Introduction

Silicon democratization is a key objective of large *Chips Acts* launched worldwide in response to the skill shortage in very-large-scale integration (VLSI) design [1, 2, 3]. An open-source (OS) hardware design approach [4, 5] is key to achieving silicon democratization, as it enables large cohorts of students to gain access to technology process design kits (PDKs), electronic design automation (EDA) tools, and design intellectual properties (IPs), which are required assets for chip design. The OS approach can facilitate innovation, as students with hands-on experience can easily transition from school to industry or start-ups.

The current status quo for VLSI courses is to focus on teaching a theoretical understanding of the design and fabrication process [5]. Those featuring practical lab modules often only *emulate* the application-specific integrated circuit (ASIC) design flow using field-programmable gate arrays (FPGAs) [5].

OS eases a more aggressive hands-on approach to teaching VLSI. *Edu4Chip* [5] targets a strong multinational undergraduate-level chip design course, teaching the theoretical background and offering hands-on experience for $\geq$ 250 students annually. This course uses *Didactic-SoC* [5], a chip platform created with *Kactus2* using *IP-XACT* descriptions. It features a *staff* section containing a RISC-V system-on-chip (SoC) and multiple *student* sections. At the time of writing, their platform neither features a synthesis nor implementation flow and heavily uses generated code, steepening the learning curve for students.

With *Croc* [6], we provide a more mature platform based on production-ready, industry-proven IPs, featuring a simple and proven physical implementation flow with supplementary exercises and lecture notes. Students gain hands-on experience on a mature set of IPs that helps bridge the gap between teaching and industry. By minimizing the size of the RISC-V microcontroller (MCU), we allow students to work on their own ASIC end-to-end, giving them complete control over the entire design and implementation. To reduce the barrier to entry, we rely solely on well-documented, parameterized, and silicon-proven *SystemVerilog (SV)* code and a streamlined implementation flow.

In November 2024, two bachelor students successfully taped out *MLEM* [7] to demonstrate Croc's implementation feasibility in *IHP*'s open 130-nm node [8].

Starting in spring 2025, ETH Zurich's ASIC design course, *VLSI2*, switches to an end-to-end OS flow using Croc. All teaching material is released under a *Creative Commons* license. [1]

We present the following contributions:

- An education-focused, extensible ASIC platform featuring a minimal RISC-V MCU implemented with silicon-proven production-ready SV IPs.
- A streamlined and documented OS EDA synthesis and implementation flow based on our work shown at IWLS 2024 [9] and our newly developed *yosys-slang* [2] SV frontend for *Yosys*.
- A successful end-to-end open IHP 130 nm demonstrator tapeout in November of 2024, silicon-proving the SoC platform for educational courses.

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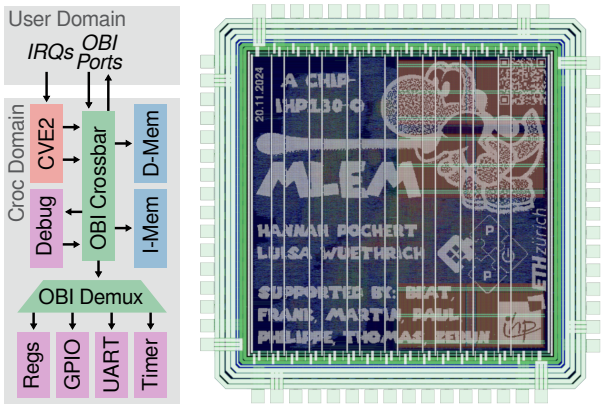

(a) (b)

Figure 1: *(a) Architecture Croc, (b) MLEM's layout.*

Croc Platform

The supporting *Croc* domain contains an OS, industry-maintained, production-ready, Ibex-based [10] *CVE2* [11] RISC-V core, a minimal set of peripherals, and an *OBI* [12] crossbar. The Croc domain primarily aids the students in implementing, debugging, and verifying their designs. Students may modify it by, for example, by implementing custom instruction set architecture (ISA) extensions or modifying the interconnect. Croc features a single-cycle tightly coupled interconnect and two SRAM banks, allowing CVE2 to achieve its ideal performance of one instruction per cycle. The *user domain* provides an interface for loosely coupled accelerators, peripherals, or experimental RISC-V cores; see Figure 1a. Croc is available ready to use from a single repository [3] with the register transfer level (RTL) description, software setup, and documentation.

We target IHP's 130 nm open PDK [8] with a fully OS design flow using *Yosys* for synthesis, *OpenRoad* to implement the backend, and *Verilator* for RTL simulation. Croc's flow is a streamlined version of our previous *IWLS 2024* [9] flow. Most notably, we replaced the complex RTL preprocessing step with our newly developed *slang-based* SV frontend for Yosys [4]. The *IIC-OSIC-TOOLS* [13] container provides the OS EDA tools and the PDK. We provide an FPGA flow targeting *Digilent*'s *Genesys 2* to support accessible, low-cost verification and emulation.

MLEM Student Tapeout

In their Bachelor's thesis, two students took the lead in extending Croc with an optimized *UART* peripheral and a *NeoPixel* [14] controller, culminating in the successful tapeout of our demonstrator chip MLEM, presented in Figure 1b. Using a predecessor of the new VLSI2 exercises, they independently designed, implemented, and verified their designs, completed the physical design flow in eight weeks, and contributed their experiences to our shared knowledge base.

MLEM measures 5 mm^2 and has a design complexity of 350 kGE at a global density of 56 %. MLEM can be implemented on a 6^{th} *Generation Intel Core i7* machine in less than one hour with a memory footprint of less than eight GiB. Of the 48 I/O pads, 12 are used by the Croc domain. The remaining 36 pins carry NeoPixel, UART, and 26 GPIOs. Under typical conditions, the design achieves a top clock speed of 80 MHz (58 logic levels) at a core voltage of 1.2 V.

Conclusion and Outlook

We present Croc, an education-focused, extensible end-to-end OS RISC-V MCU platform built around mature, silicon-proven SV IPs used in multiple commercial projects and industry-supported repositories. Croc thus bridges the gap between teaching and industry, allowing the students to use this platform as a starting kit to develop commercial RISC-V MCU products, e.g., for security, control, or edge machine learning applications. Croc comes bundled with a comprehensible OS EDA synthesis and implementation flow together with educational material to build physical implementation experience. We successfully taped out MLEM, establishing Croc as the ASIC platform for our VLSI2 course. In 2025, VLSI2 will educate approximately 80 students at ETH alone, producing up to 40 OS ASIC layouts and up to five SoC tapeouts using IHP's 130 nm PDK.

Acknowledgment: This work was supported through the SwissChips Initiative. Silicon is funded by the German BMBF project FMD-QNC (16ME0831).

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