Croc: An End-to-End Open-Source Extensible RISC-V MCU Platform to Democratize Silicon

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Croc repo

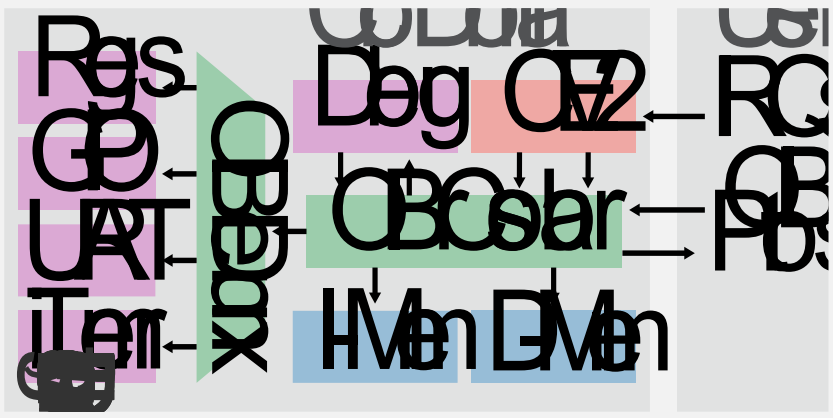
1 Motivation

- **Silicon democratization** is a key objective of "Chips Acts"[1,2]
  - Addresses **shortage of skilled chip designs** worldwide
  - **Requires open-source hardware platforms** with accessible PDKs, EDA tools and design IPs[3]
- **Hands-on ASIC education** offers benefits:
  - **Practical experience** along theoretical teaching
  - **Broad access** and deep integration into courses
  - **Quick entry** and silicon-proven **SystemVerilog** IPs
- **Facilitate innovation** with hands-on ASIC experience
  - **Student-led experimentation** made easy and encouraged
  - **Eases transition** to industry or startups

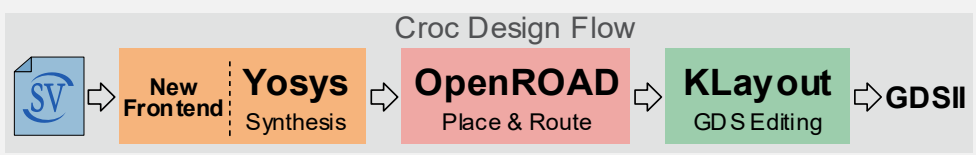
Croc is a tapeout-proven education platform with open course material and a well-documented design flow

2 Croc Architecture

- The **Croc domain** aids students during design and testing
  - CVE2[4], a **production-ready RISC-V core** based on Ibex
  - **Minimal peripherals** to ease debugging
  - **OBI-crossbar** as a simple and extensible interconnect
  - **Single-cycle SRAM** banks to achieve ideal CPI

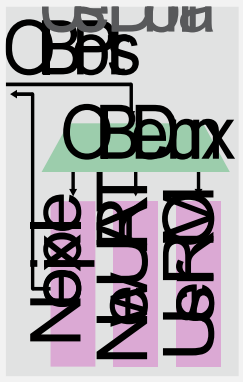


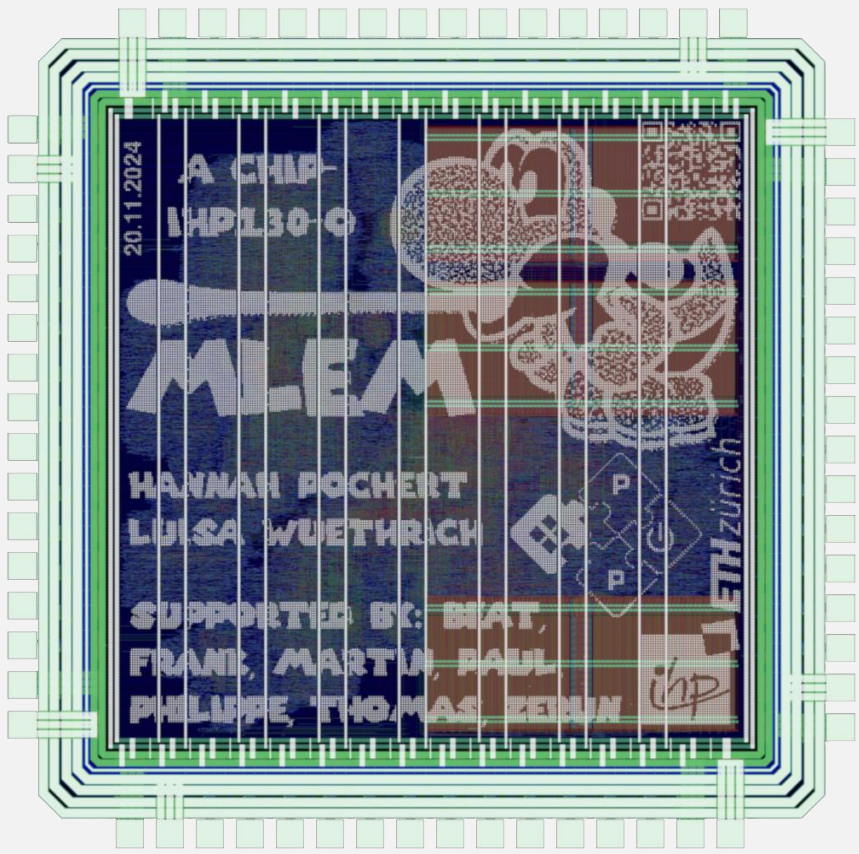
- The **User domain** as a starting point for custom IPs
- **Croc's design flow** is simple and documented
  - Newly developed slang-based **SystemVerilog frontend**
  - **IIC-OSIC-TOOLS container**[5] eases installation, deployment and use on any desktop OS



3 MLEM Student Tapeout

- **First tapeout completed** in November 2024
  - Two **Bachelor students** finished tapeout
  - **UART and Neopixel peripherals** developed, tested and integrated into Croc
- **MLEM implemented in IHP 130nm**[6]
  - 48 digital IOs, **5mm²** (350 kGE)
  - Signoff at **80MHz** @ 1.2V (tt-corner)





4 Conclusion

- Croc is an **education-focused, extensible end-to-end open-source hardware platform**
- The **minimal SoC** is built around **mature SystemVerilog IPs** used in commercial projects
- The **MLEM student chip** shows Croc potential as a **complete platform for hands-on ASIC courses**

VLSI 2 course

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