CVA6 Design Space Exploration on Agilex™ 7 FPGA

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CVA6 CONFIGURABILITY: A BENEFIT AND A CHALLENGE

CVA6 offers a wide range of configuration parameters that permit to design a variety of cores: from solutions for applications with Linux support to embedded processors running bare-metal applications. While this offers great flexibility, it also brings the challenge to choose the best configuration for a new design, making it difficult to know where to start from, or which are the right choices to make.

PORTING & OPTIMIZING CVA6 ON ALTERA™ FPGA

CVA6 was initially designed for ASIC targets, but the interest to have a vendor-independent FPGA version emerged, resulting in the FPGA configuration in CVA6 repository.
The existing configuration is optimized for Xilinx FPGAs (now AMD). The current work optimizes CVA6 for Altera™ FPGAs.

1) Porting the technology specific optimizations to Altera™ technology: Altera™ and Xilinx support different primitives, so some of the optimizations used for Xilinx FPGAs can't be reused in Altera™ (e.g. asynchronous RAM)
2) Creating a design equivalent to the Xilinx Application Processing Unit (APU) for Agilex™ 7 platform.

DESIGN SPACE EXPLORATION

We start with the FPGA configuration as is (A), and explore what is possible in terms of performance and reduction of resources, focusing on embedded configurations.

EXPLORED CONFIGURATIONS

A	OpenHW FPGA config. without Xilinx FPGA optimizations
B	Altera™ FPGA optimizations enabled
C	No MMU
D	B + C + best cache performance*
E	D + no privilege levels
F	E + only C extension (remove Zcb, A, B , Zicond)
G	F + store and commit buffer depth 2
H	G + reduced cache**
I	H + 2 scoreboard entries
J	I + one single load buffer entry
K	J + SRAM instead of DDR
L	H + SRAM instead of DDR

*best cache performance: 16 KB cache, 512 bits cache line and 4 ways. Same for Data and Instruction caches.
**reduced cache: cache line of 64 (width of AXI bus), with only 1 way. 8KB instruction cache, 4KB data cache.

RESULTS

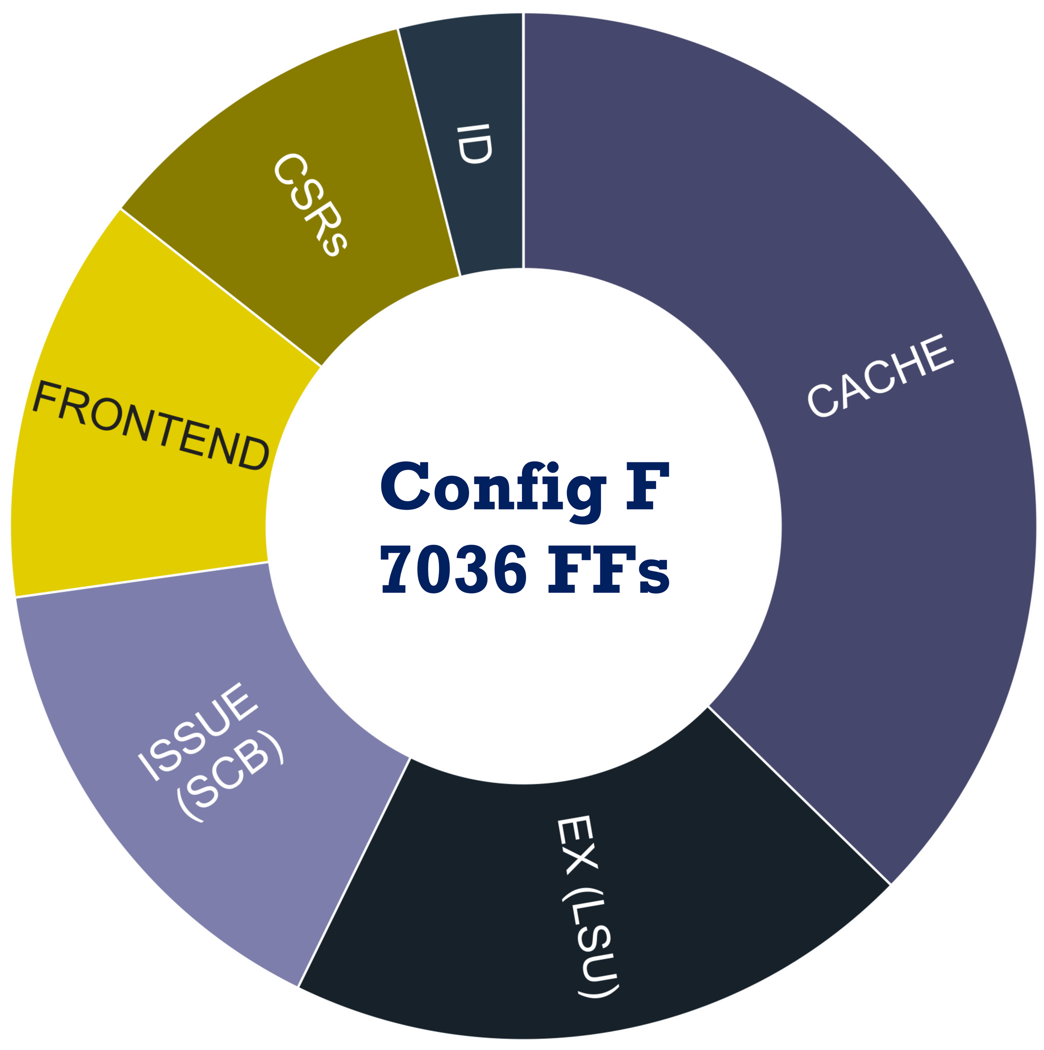
PERFORMANCE

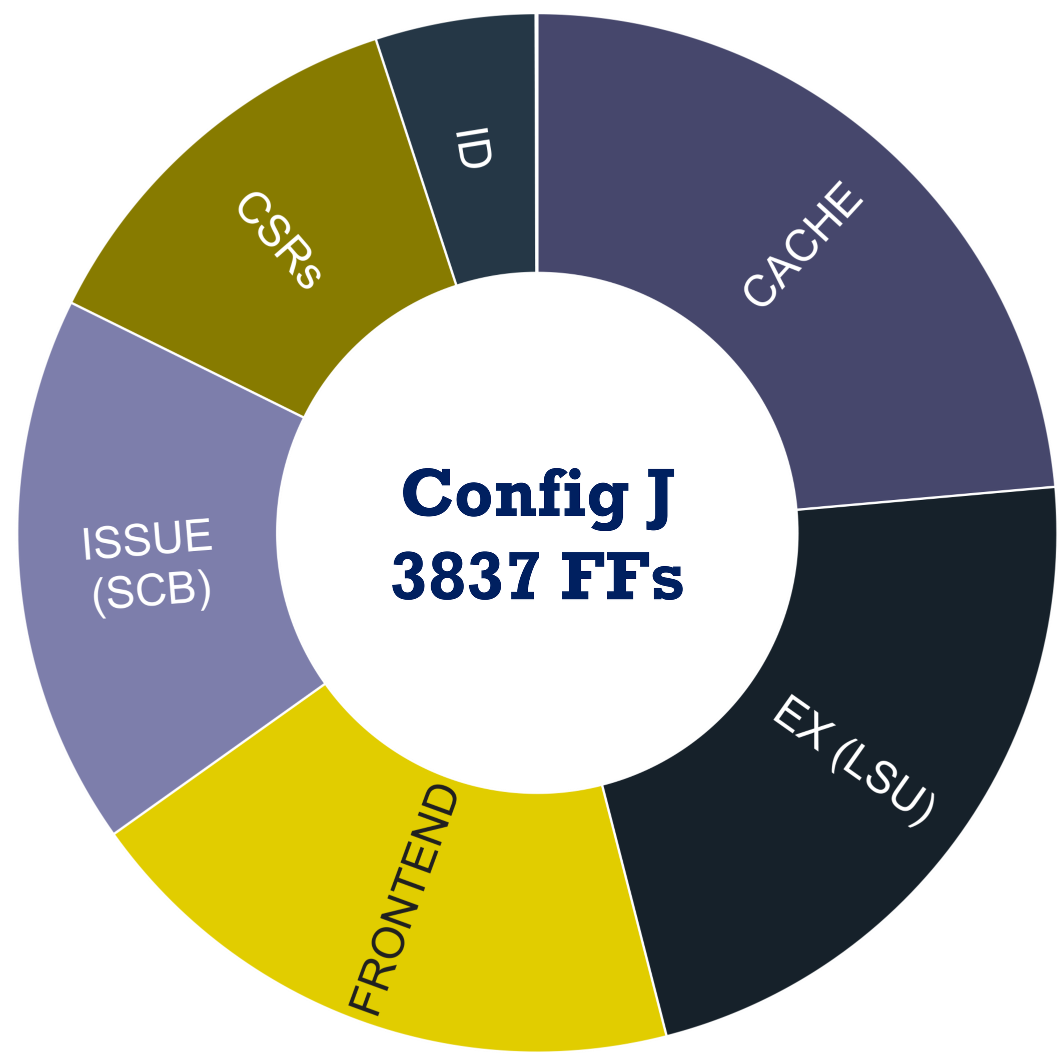
	Coremark/ MHz	Fmax (MHz)	Coremark Total	
A	2.00	200	400	
B	2.00	215	430	+7%
C	2.00	215	430	+7%
D	2.30	215	498	+25%
E	2.30	217	499	+25%
F	2.30	218	501	+25%
G	2.25	220	495	+24%
H	1.90	220	418	+4%
I	1.50	220	330	-17%
J	1.50	220	330	-17%
K	1.80	210	378	-5%
L	2.50	210	525	+31%

RESOURCES

	LUTs		FFs		BRAM	
A	12,530		8,959		24	
B	11,621	-7%	5,874	-34%	32	+33%
C	11,411	-9%	7,908	-12%	20	-16%
D	15,773	+26%	7,521	-16%	135	+462%
E	15,591	+24%	7,409	-17%	135	+462%
F	13,738	+10%	7,036	-21%	135	+462%
G	13,823	+10%	6,650	-26%	135	+462%
H+L	7,710	-38%	4,422	-50%	16	-33%
I	7,150	-43%	3,874	-56%	16	-33%
J+K	7,273	-42 %	3,837	-57%	16	-33%

DISTRIBUTION OF FFs





KEY RESULTS

- FPGA optimizations successfully ported to Altera™ technology → reduce 34% of FFs
- Frequency optimizations offered by Quartus® → up to 220 MHz (started at 175 MHz)

- Best performance result is achieved with biggest cache → memory access as bottleneck
- After cache, the biggest resources consumption is in the LSU → performance tradeoff
- After LSU, the biggest resources consumption is in the Scoreboard → performance tradeoff

- Change APU design to use SRAM instead of DDR → decouple CVA6 performance from memory architecture

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