Efficient Trace for RISC-V: Design, Evaluation and Integration in CVA6

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Motivation and Contributions

- Traditional profiling techniques involve **significant trade-offs** between being intrusive and offer detailed debugging [1]. **Instruction Branch Tracing** allows continuous profiling by tracking the **program counter (PC) address deltas** introduced by discontinuities.
- This work presents three main **contributions**: i) The design of a **Tracing System** compliant with the **RISC-V E-Trace specification** [2]; ii) Its **integration** into a modern RISC-V edge platform based on the **CVA6 core** [3]; iii) The **evaluation** of the proposed implementation in terms of achieved **average compression rate** and **FPGA resource utilization overhead**.

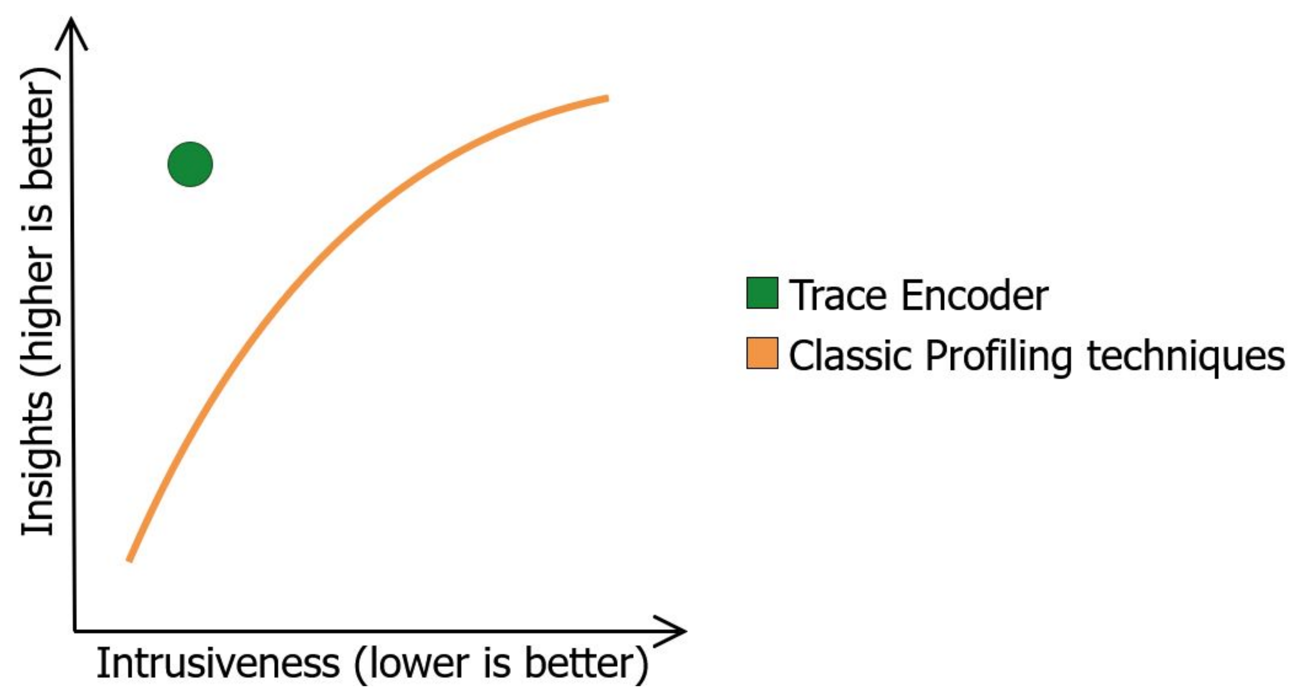

Fig. 1: Comparison of Trace Encoder and classic profiling techniques.

Design and Integration

- The **Trace Encoder** (TE) has the following **internal modules** that implements its functionalities: **te_filter**, **te_priority**, **te_packet_emitter**, **te_reg**, **te_branch_map**, **te_resync_counter**.
- To make the TE communicate with a CVA6 core, it is necessary an interface module, the **Trace Interface Port** (TIP) that translates CPU signals into TE intelligible signals. To extract the TE output - the packets - via **AXI** an **Encapsulator** is necessary.

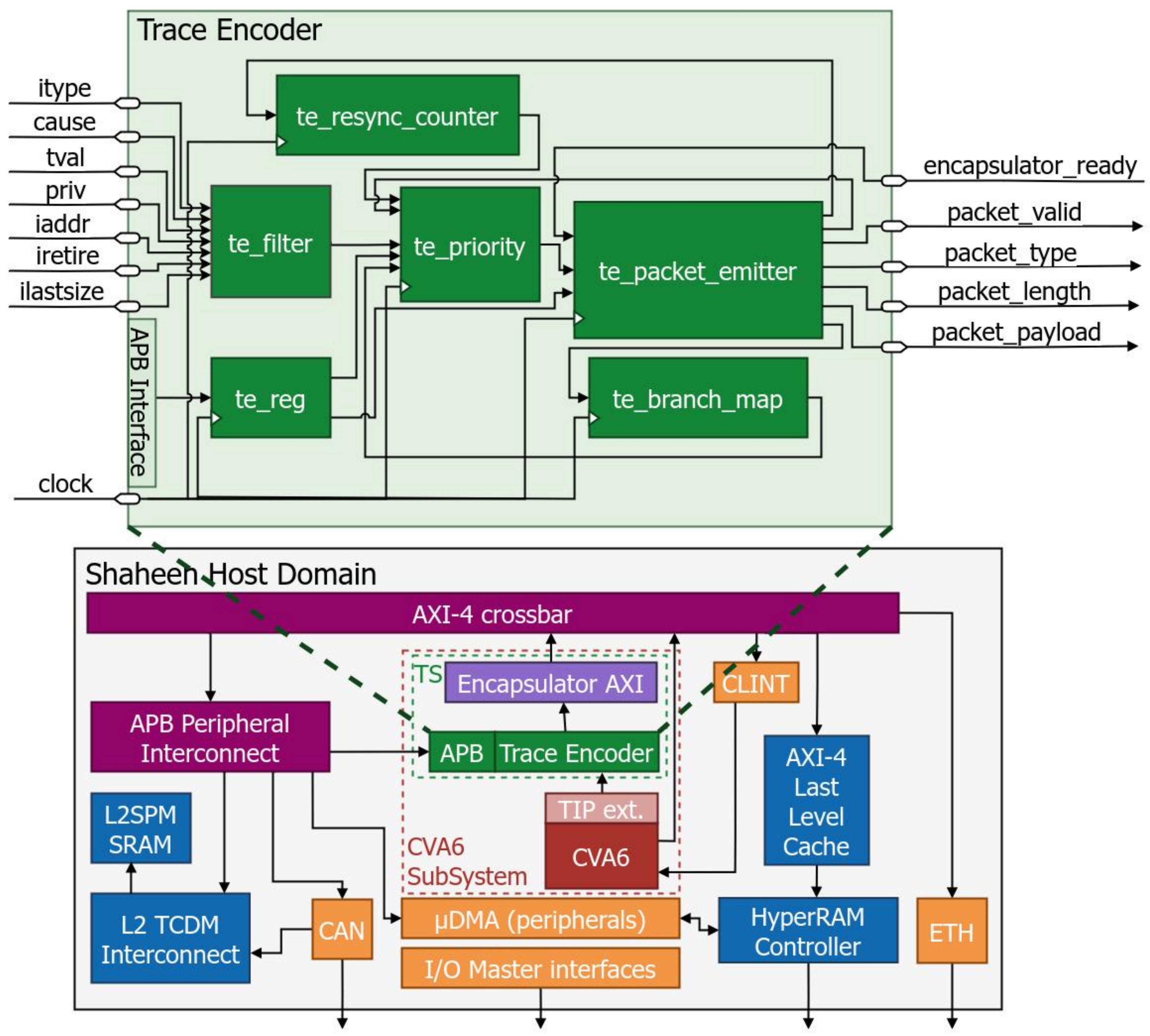

Fig. 2: Trace Encoder internal architecture and integration within Shaheen.

Results and Future Developments

- The whole **Tracing System** (TIP, TE, Encapsulator) occupies around **10% of the area occupied by a CVA6 core**. The **average compression rate** w.r.t the uncompressed instruction obtained by the TE is **95.1%**.
- In the future the TE can be extended to **implement other functionalities** to further increase the average compression achieved. Currently, a **Trace Decoder** to reconstruct the trace from the packets emitted by the TE is **in development**.

Test name	Compression rate %
axi_hyper_fibonacci	99.8
bypass_cva6_dco	99.5
can	87.3
dhrystone	98.4
fp16_matmul	99.7
fp16-vec_matmul	99.7
hello	90.4
kmeans	95.0
l1_test	99.7
llc_spm_test	87.6
mbox_test	91.7
mm	99.7
sb_macl_444	99.7
sb_macl_844	99.7
timer	85.2
Average	95.1

Tab. 1: Achieved compression rate in platform specific tests.

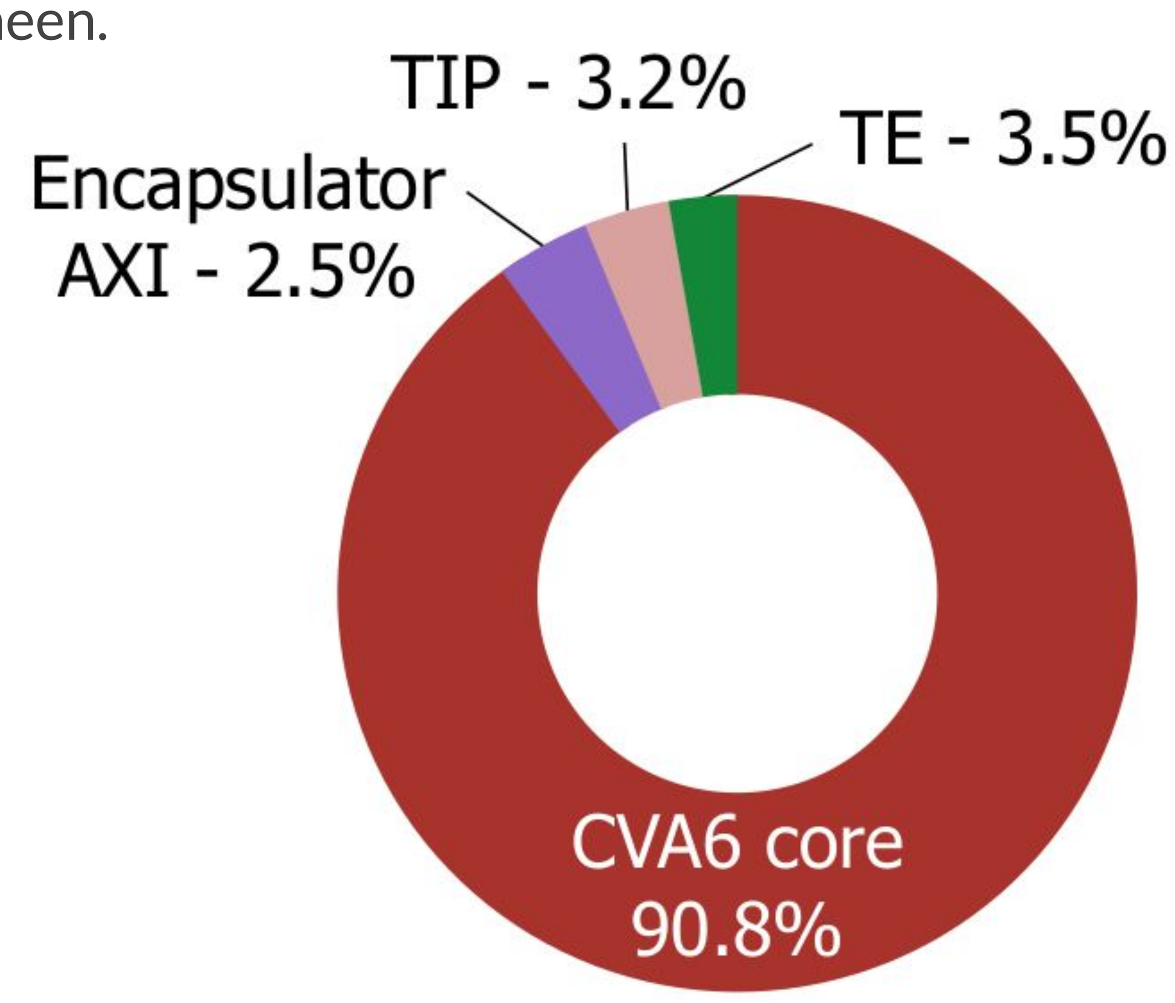

Fig. 3: Tracing System area usage w.r.t a CVA6 core.

[1] Charlie Curtsinger et al. "Coz: Finding code that counts with causal profiling". In: Proceedings of the 25th Symposium on Operating Systems Principles (2015).
[2] Gajinder Panesar et al. "Efficient Trace for RISCV". In: Siemens, ver. 1.1. 3-Frozen (2022).
[3] Luca Valente et al. "A Heterogeneous RISC-V Based SoC for Secure Nano-UAV Navigation". In: IEEE Transactions on Circuits and Systems I: Regular Papers (2024).

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