Embedded FPGA-Shell: Emulating RISC-V Architectures at FPGA

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MOTIVATIO N

✅ **FPGA validation is essential for RISC-V processor development and system-level research.**

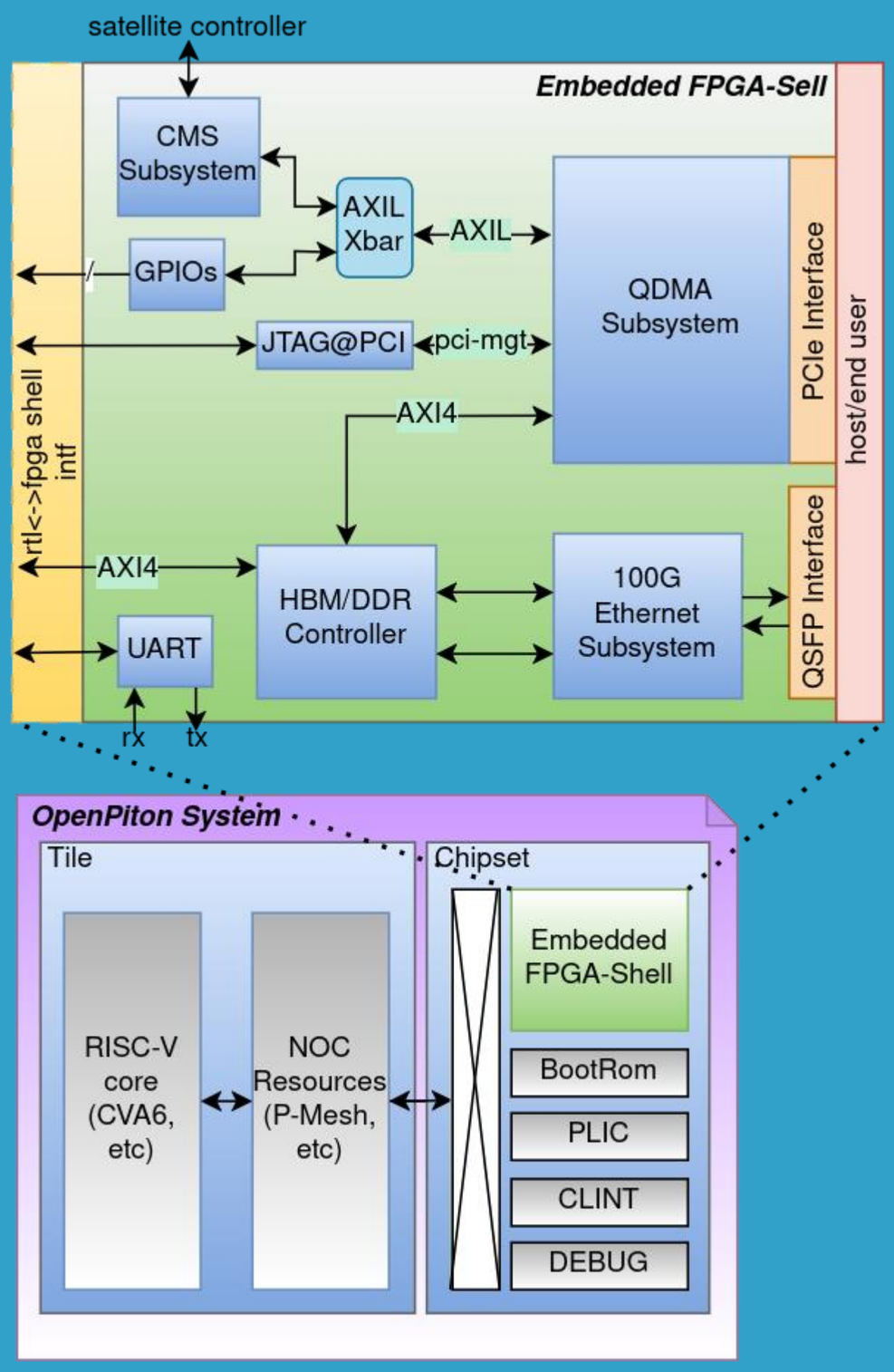
🧩 **Developers spend excessive time wiring up interfaces (PCIe, DDR, JTAG, etc.) rather than focusing on core architecture.**

🛠️ **Lack of reusable, modular shells makes porting to new FPGA boards difficult and time-consuming.**

🔄 **Debug and bring-up processes are fragmented across toolchains and scripts.**

💡 **We introduce an open-source, plug-and-play FPGA shell to automate and streamline the emulation of RISC-V multicore designs on AMD platforms.**

EMBEDDED FPGA-SHELL



fig#1: Embedded FPGA-Shell architecture integrated with OpenPiton system

ARCHITECTURE

🧱 **Shell Structure**:

- Modular design combining IP blocks, scripts, and integration interfaces.

🔌 **Integrated Peripherals**:

- QDMA (PCIe), Ethernet (QSFP), DRAM (DDR4/HBM), UART, JTAG@PCIe, QSPI Flash, CMS.

📎 **System Integration**:

- Connects directly to OpenPiton's chipset (AXI4/AXI-Lite interfaces).
- Supports CVA6 and in-house designed RISC-V cores.

🌐 **Communication & Interconnect**:

- AXI crossbars for IP integration.
- Aurora (FPGA-FPGA link), PCIe (host communication).

FPGA-TOOLS

📂 **Project Automation**

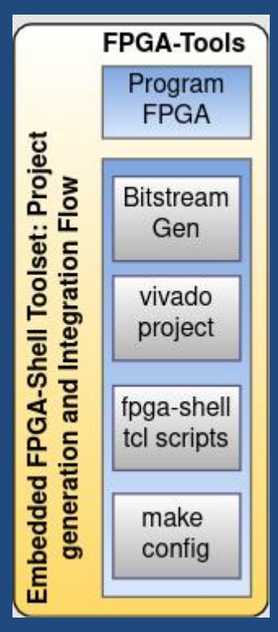
- **Makefile-based config & build flow**
- **Automates project setup, synthesis, and bitstream generation**

🛠️ **Vivado Integration**

- **Custom TCL scripts for block design and IP configuration**
- **Supports both UltraScale+ and Versal architectures**

💻 **Debug Toolchain**

- **JTAG@PCIe with OpenOCD**
- **Dual-level debugging (OpenPiton**



fig#2: FPGA-Tools

EVALUATION

- Emulated in house and open source Multi Core RISC-V designs.
- Multistage Linux boot verified.
- Performance evaluation (in progress)

IP	LUTs (1303680)	CLB Regs (2607360)	BRAM Tile (2016)
QDMA	49887	51468	81.5
HBM	1073	874	4
Ethernet	47965	68861	29.5
Others	2650	3549	0

This paper is co-financed by the Barcelona Zettaescale laboratory which is financed by the Ministry for Digital Transformation and of Public Services, within the framework of the Resilience and Recovery Facility

PARTNERS

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Project Link