The Architecture of Intelligence:
Delivering the future of computing from the Data Center to the Edge

Andrea Gallo
9th June 2026

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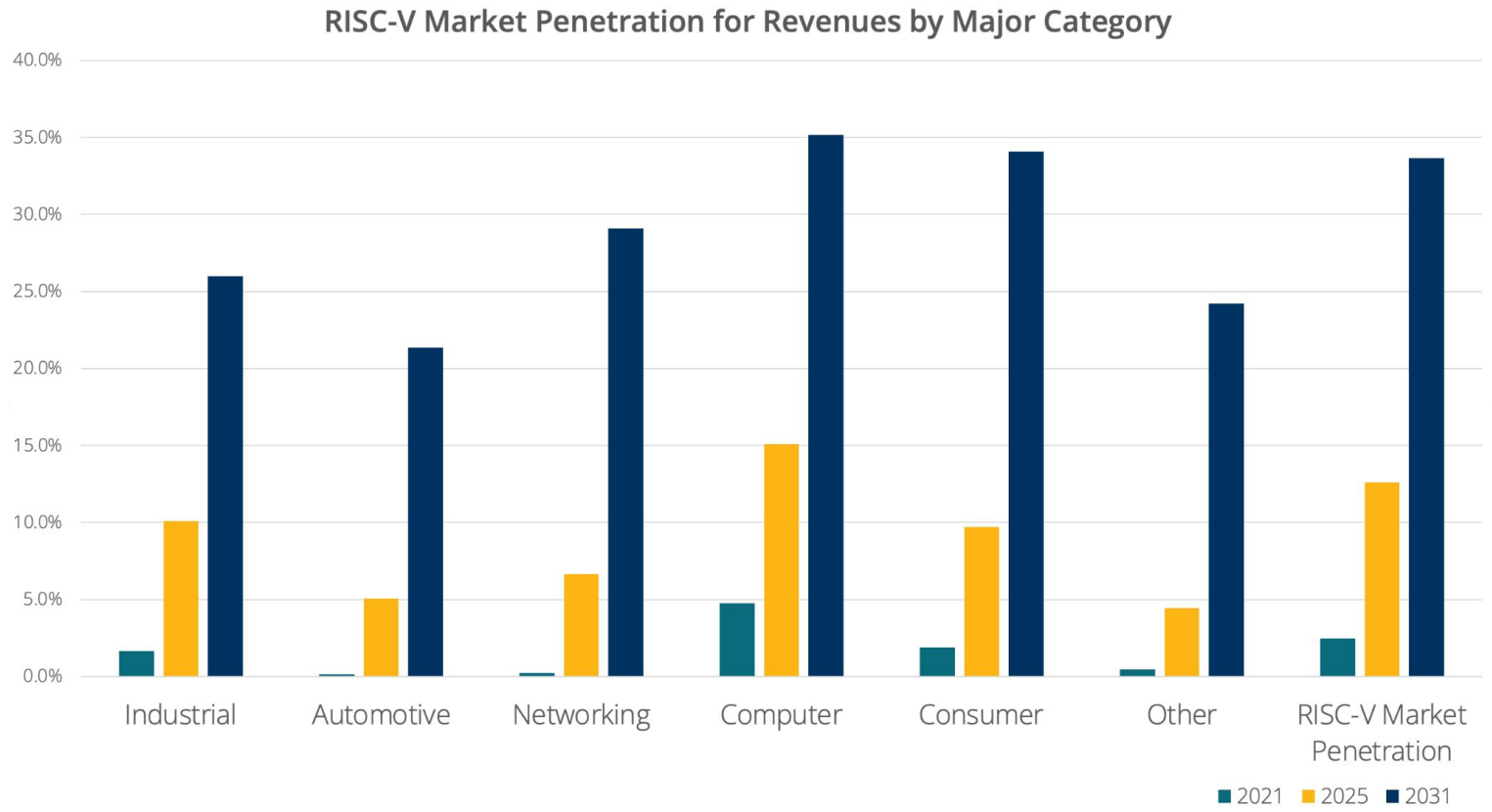
Gold Sponsors

RISC-V is the Architecture of Intelligence

RISC-V®

From 2.5% to 33.7% in 10 years!



the SHDgroup

RISC-V®

Investors believe in RISC-V

SiFive Raises $400 Million to Accelerate High-Performance RISC-V Data Center Solutions

Dutch AI inference chipmaker Axelera AI raises $250M

New Strategic Members

CARIAD
A VOLKSWAGEN GROUP COMPANY

ECP Pro GmbH

Epic Semi

hitex

NEXTSILICON

MIDSTALL

RED semiconductor

MetaStone 元石智算

OmniTrust

九望科技 VSAI

LECARC

Matt Perry

Vice President, BD & Strategic Partnerships, Azure Silicon & HW Systems

Ken Dockser

Senior Principal Architect

Delivering the future

Automotive

Infineon

Adds RISC-V tools to DRIVECORE

MIPS a GlobalFoundries company · Green Hills SOFTWARE

Accelerate Safety Certified Product Development

QUINTAURIS

team up with eSOL on RISC-V auto software integration

FuSa whitepaper coming soon
Automotive Special Interest Group

Embedded / IoT

ESPRESSIF

ESP32-S31 Dual-Core RISC-V SoC with Wi-Fi 6, Bluetooth 5.4

UpbeatTech

World's Smallest AI-Powered MEMS Vibration Sensors

DFROBOT DRIVE THE FUTURE

HUSKYLENS 2, Advancing AI Vision Education

Work in progress to define a microcontroller profile RVM

Space

MICROCHIP

NASA Next-Gen High Performance Spaceflight Processor Testing

FRONTGRADE Gaisler · Funded by the European Union

European Commission "COSMIC7" RISC-V 7nm Microprocessor for Space

BREKER™ · FRONTGRADE Gaisler

Collaborate on High-Reliability RISC-V Fault Tolerant Processor Core

Space Special Interest Group formed

Security

SEAL SQ semiconductors + quantum

QS7001 Quantum-Ready Hardware RoT with RISC-V Core

Linea

Announced its adoption of RISC-V for its Ethereum Layer 2 project

Technical University of Munich

QUASAR-CREATE, involving TUM, aims to develop the world's first fully open-source PQ-secure RISC-V processor system

Security whitepaper: TEEs Using RISC-V Supervisor domains

CHERI standard under development

RISC-V®

AI

tenstorrent

Unveils TT-QuietBox(TM) 2 Workstation for Teraflop-Class Inference

XUANTIE

Launches XuanTie C950 CPU targeting Agentic AI

semidynamics

Announces Strategic Cooperation to Develop EU-Sovereign Rack-Scale AI Compute Platform

IME, AME and VME in development

Data center

ANDES

Phison Selects Andes RISC-V Cores for its First aiDAPTIV+ AI Solution for edge and data center

InspireSemi™ E4 COMPUTER ENGINEERING

Thunderbird™ “supercomputer cluster-on-a-chip” accelerated computing platform

希姆计算 STREAM COMPUTING

China Mobile RISC-V thousand-card computing cluster successfully deployed with 150 PFLOPS

RISC-V®

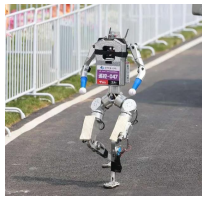
UEFI ACPI 6.6 added official support for RISC-V

Server SOC and Boot Requirement specifications ratified

Consumer

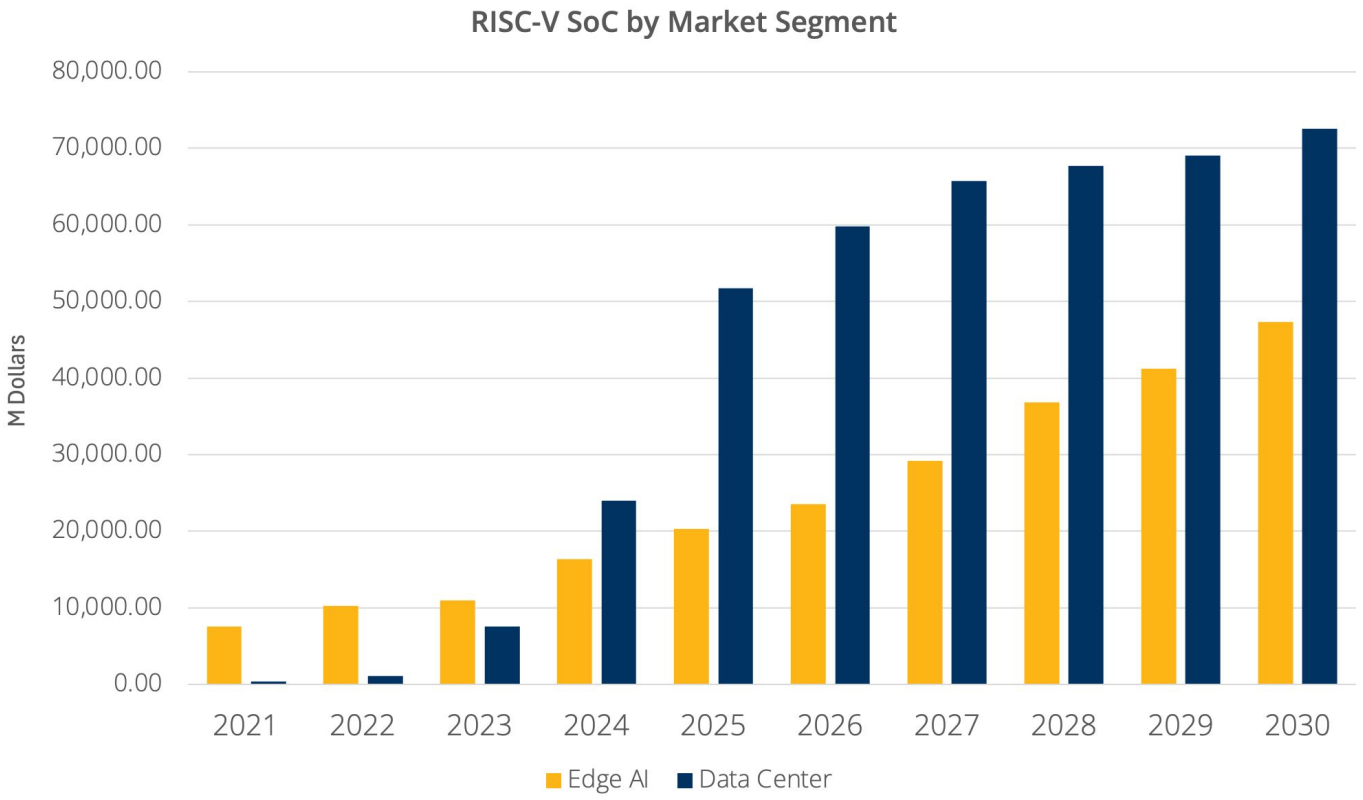
Xteink X4 Ultra-thin Magnetic Back eReader based on the ESP32-C3 from Espressif Systems

RISC-Y, is a custom game console RISC-V SoC implemented on the Sipeed Tang Nano 20k board housing the Gowin GW2AR-18 FPGA.



Linglong 2.0 robots, based on SpacemiT K3, successfully complete Beijing Yizhuang Humanoid Robot Half Marathon

The Rise of RISC-V in Edge AI and Data Center



the SHDgroup

RISC-V®

A rich ecosystem of **Software**

High performance **Silicon**

Versatile and extendable **ISA specs**

RISC-V®

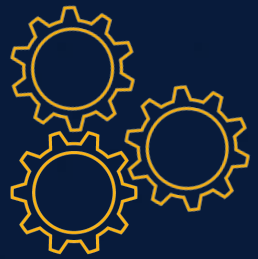
Specialization from **Platforms**

Standardization through **Profiles**

An extendable base **ISA**

RISC-V®

Announcing Server Platform Specification 1.0



Interoperability and Compliance to Industry Standards

RAS

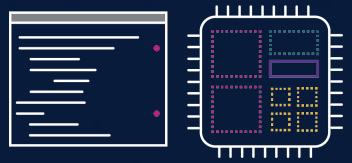
Security

Performance

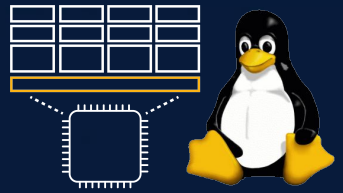
Quality of Service

RISC-V®

Announcing Server Platform Specification 1.0

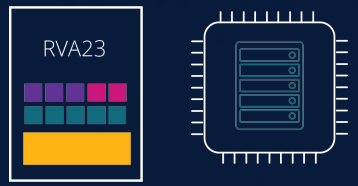


Industry Standard boot architecture and runtime services



Portable system software can rely on the platform

Interoperability between conforming servers and portable system software



Built on top of RVA23

RISC-V®

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RISC-V®

2026 is the year of the RVA silicon

SiFive Performance™ P870D and P570

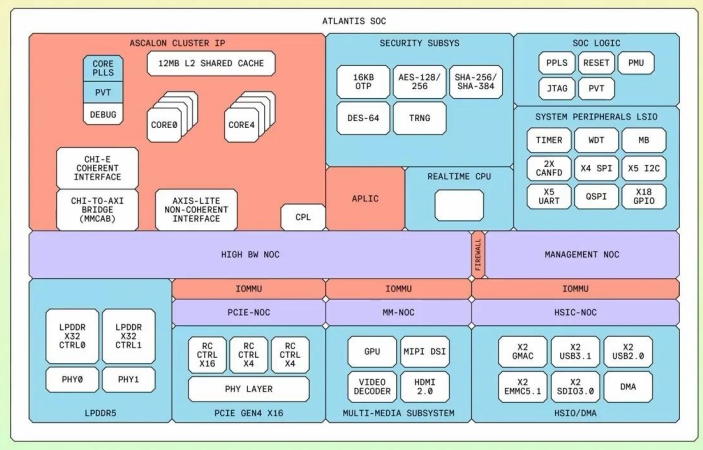
- P870D already taped out and already in a customer's server chip today
- **RVA23** true server class, RAS, DVFS, System IP, IOMMU, WorldGuard, Virtualization, Trace and Debug, up to 128 cores

- P570 Gen3 purpose-built for demanding edge AI, high-end consumer, and commercial IoT
- **RVA23** application processor with single vector processing unit capable of handling parallel operations, including dot products, with 2 x 128-bit vector registers, support for BFloat16

Atlantis platform

tenstorrent

- Compute platform and development board
- Optimized for HPC, robotics, automotive, and edge AI applications
- 8-core Ascalon X CPU cluster based on the **RVA23** profile
- Atlantis supports the Ubuntu operating system
- Designed for comprehensive ecosystem enablement
- SoC and board bring-up is on track for Q4 2026



EPIC Contrail AIX

RISC-V Artificial Intelligence eXecution Platform

- Server class RISC-V compute and AI acceleration
- Single unified CPU + AI superchip
- Silicon and server platform available now

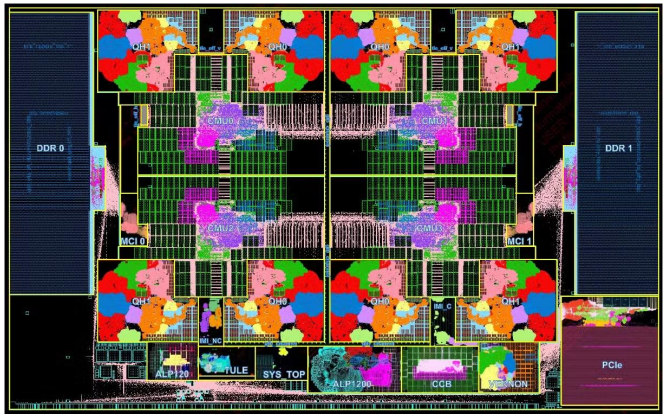
Contrail Compute Features

- **RVA23** RISC-V architecture
- 32 RISC-V scalar processor CPU cores
- 16 Integrated AI acceleration RISC-V cores
- Up to 75 TOPS AI processing
- DDR5 memory architecture
- PCIe Gen5
- CXL memory expansion
- Hardware virtualization
- Enterprise-grade security and reliability

Alpine Test Chip

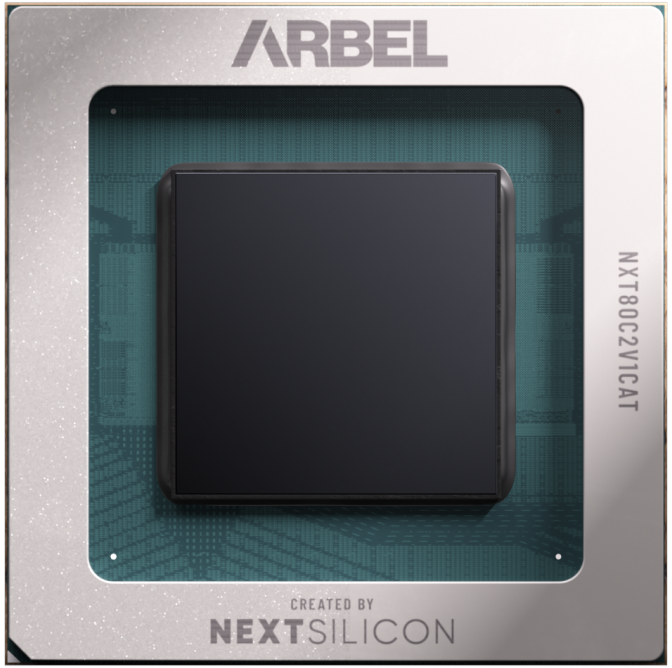
AKEANA

- Eight 64-bit, out-of-order **RVA23**, server class cores
- 64-bit in-order core, 4-way simultaneous multi-threaded, 512b vector engine
- 32-bit in-order cores for system management, security, and real-time applications
- Taped out December 2025
- Alpine Software Development Board available second half of 2026



RISC-V

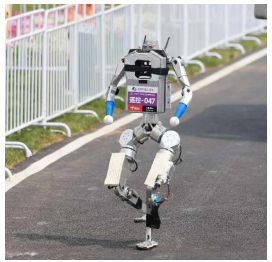
NextSilicon



- Maverick-2: The industry's first Intelligent Compute Architecture (ICA) for AI and HPC workloads.
- Delivers performance at scale for the most demanding HPC applications while consuming up to 60% less power than traditional GPUs.
- Arbel: NextSilicon's server-grade RISC-V CPU, designed for next-generation AI and HPC workloads.
- **RVA23** news following soon – including an exclusive announcement on Wednesday at the Summit.

SpacemiT K3

- 8 **RVA23** compliant X100 Cores:
  - 4-issue out-of-order execution
- 8 A100 AI Cores:
  - Supports up to 1024-bit RVV1.0
- Up to 60 TOPS of AI performance
- Deployed across applications from robots to servers
- SpacemiT donated 15 boards to RISC-V Developer Program



SpacemiT K3 servers hosted by Scaleway

RISE
RISC-V Software Ecosystem

Canonical

Scaleway

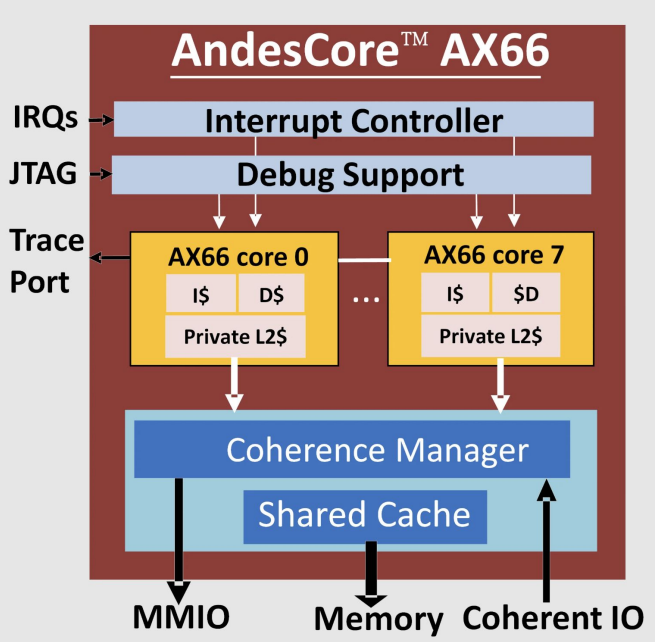
SPACEMIT

- Spacemit, Canonical, Scaleway, and RISE collaborate to stand up **RVA23** servers based on K3
- Available to software projects across the ecosystem through RISE managed GitHub runners and direct SSH access
- Enabling work on llama.cpp, Kubernetes, k0s, k3s, PyTorch, NumPy, OpenBLAS, ExecuTorch, and many others
- Expected online end of June!

XiangShan-Powered Server Chip

- SPACEMIT V100 Server Chip based on XiangShan
- Full compliance with the RISC-V **RVA23** profile, RISC-V Server SoC Specification, and Boot and Runtime Services (BRS) Specification
- 6 XiangShan Kunminghu cores
  - 16.5/GHz on SPEC CPU 2006 Integer
- 40 in-house SpacemiT X100 cores

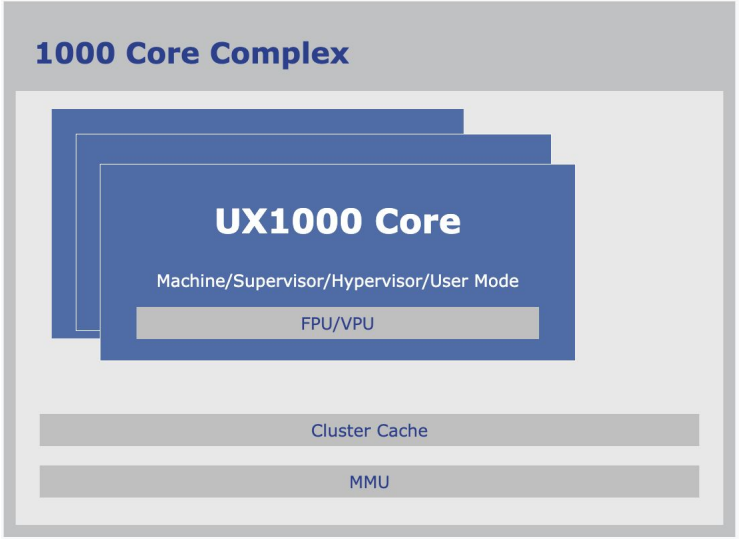
AndesCore AX66



- Andes is ready to welcome RISC-V Silicon for **RVA23**
- 64-bit out-of-order 4 wide decode 13-stage CPU core
- Symmetric multiprocessing up to 8 cores
- Target applications
  - Networking and Communications
  - Android Devices
  - Video and Multimedia Processing
  - SmartNIC or DPU
  - AI SoC
  - Edge Servers

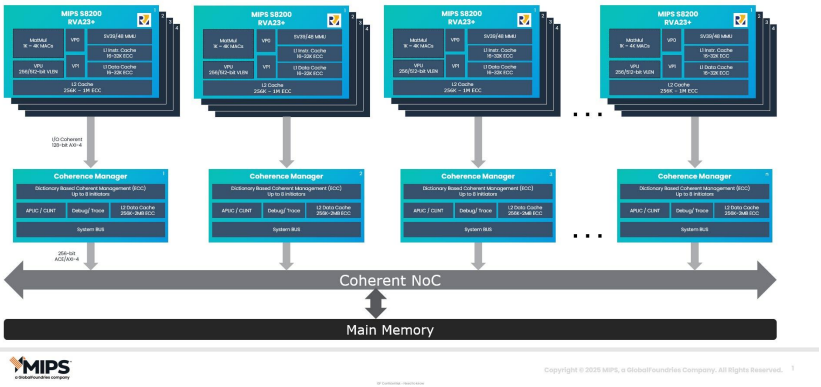
Nuclei UX1030H

芯来科技 NUCLEI



- Server, Android, ADAS and robotics applications
- **RVA23** support
- From 2 - 6 issue width
- Up to 8 SMP cores in one Cluster with Cache Coherency.
- Configurable Private L2 cache + Cluster Cache

MIPS S8200



- Software-first RISC-V NPU enables Physical AI at the autonomous edge
- The award-winning MIPS S8200 RISC-V NPU delivers support for modern AI models at the edge, increased efficiency, and performance improvements using an open, scalable architecture
- Enables efficient, scalable Physical AI solutions across multiple markets
- **RVA23**

DC-ROMA RISC-V Mainboard III

DeepComputing

- The world's first **RVA23** laptop
- Powered by SpacemiT K3
- Fully compatible with Framework Laptop 13
- RISC-V performance on a modular, repairable, and upgradeable laptop platform
- SpacemiT K3, 8-core RVA23 CPU
- Ubuntu Desktop 26.04 LTS

Android 16 on RVA23

XUANTIE

- XuanTie team announced successful enablement of Android 16 (AOSP mainline code) on **RVA23**
- Running on Xuantie 9 Series high performance processors
- The XuanTie Android platform released to strategic customers
- The XuanTie Android platform is fully compatible with system specifications such as AVB, GKI, GSI, and VINTF

Ubuntu 26.04 LTS - Resolute Racoon

"Ubuntu now fully supports **RVA23**, the baseline standard for RISC-V. This ensures that teams innovating on RISC-V can take full advantage of the platform, including in mixed-architecture environments."

Long Term Support

- New release every 2 years
- Prioritises stability
- 5 years support and security updates
- 15 years of support through Ubuntu Pro
- Read more on the Ubuntu blog

A rich ecosystem of **Software**

High performance **Silicon**

Versatile and extendable **ISA specs**

RISC-V®

Coordinate

Accelerate

Upstream

RISC-V®

RISE
RISC-V Software Ecosystem

RISC-V Runners - free native CI on GitHub

- Launched March 2026
- Install a GitHub App, change one line, run CI on real RISC-V hardware
- No emulation, no waitlist
- Adopted by Llama.cpp, Kubetail, Kairos, alibaba/zvec, numpy, pytorch, k0s, and more

13K+ Workflows

~264 Repositories

~116 Organizations

Developer appreciation program

- Rewarding developers who port, test, and release on RISC-V
- Driving RISC-V as standard practice

13 Awarded

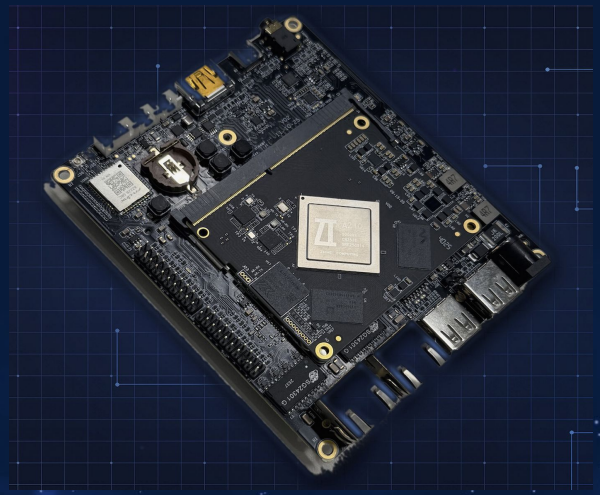
Build farm

- 7 active projects onboarded.
- Thousands of builds and millions of tests monthly.
- OpenJDK CI, toolchain fuzzers.
- JenkinsFile onboarding with GitHub/GitLab integration.


RISC-V

RISE
RISC-V Software Ecosystem

XuanTie Donating 100x A210 Boards to new RISE Board Farm



- XuanTie Donating 100x A210 Boards to RISE Board Farm
  - Quad-core XuanTie C920 + XuanTie C908
- Hosted at Oregon State Open Source Lab
- Setup in progress
- 20 boards shipped
- Pilot in Q3
- Additional boards, including RVA23 hardware added from Q4

RISC-V®

A rich ecosystem of **Software**

High performance **RVA silicon**

A versatile and extendable **ISA specs**

RISC-V®

RISC-V is inevitable

RISC-V is inevitable
It is not if but when

RISC-V is inevitable

It is not if but when

RISC-V is NOW

RISC-V®

Have a great week at RISC-V Summit Europe 2026!