

The background features a dark blue gradient. A semi-transparent, glowing cube is positioned in the center-left. From the top-right corner of the cube, a dense trail of white and light blue particles or data points extends towards the top-right corner of the frame, creating a sense of motion and digital flow.

Tailoring Workloads for Agentic AI Using Advanced Virtual Platforms for RISC-V

Sam Grove, Head of Software Tool products at MIPS by GF

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MIPS & ARC Together



Building a world leading RISC-V IP, software, and custom silicon platform



Footprint

First RISC-V company
at scale

Ecosystem

300+ customers
across MIPS + ARC

Expertise

Family of 41 different
RISC-V and AI cores

The CPU Explosion for Agentic AI

x10

IDC forecasts a tenfold increase in the number of agents within large enterprises

\$45B

Deloitte predicts global agentic AI market could reach \$35 billion in 2030. It puts the market at \$8.5 billion in 2026. The stronger orchestration of agents could lift the 2030 projection by up to 30% to \$45 billion

CPU GPU SHIFT

The CPU-to-GPU ratio shift ("training: 1:8, inference: 1:4, agentic: trending toward 1:1"), Intel earnings

AMD earnings "1:4 to 1:1 ratio shift"

In the agentic AI era, every edge MPU & MCU platform will be developed to enable Physical AI

Software-First Design to Rethink Agent AI for Edge



The movement from one-size-fits-all components to open, collaborative, adaptable silicon enables a competitive edge and faster time to market

Off-the-shelf is someone else's vision for your platform

Closed architectures limit agility and flexibility while constraining innovation

Standards-based IP inside purpose-built silicon is a collaborative approach

Software-first design drives platform optimization & reduces time to market

The “Linuxification” of Hardware

Linux Kernel Release

Select Libraries & Packages

Catalog Silicon Platform

10's of millions of products

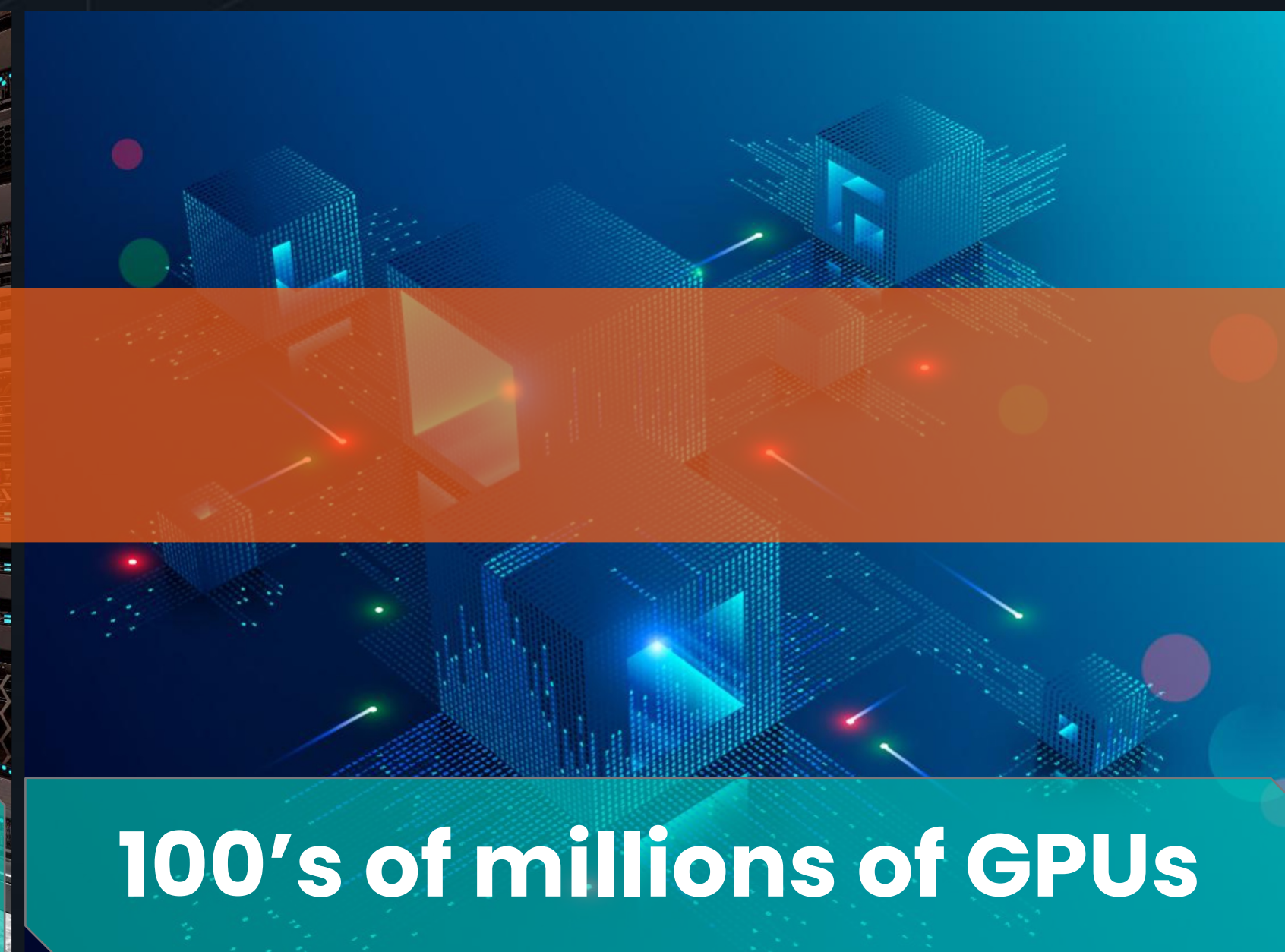
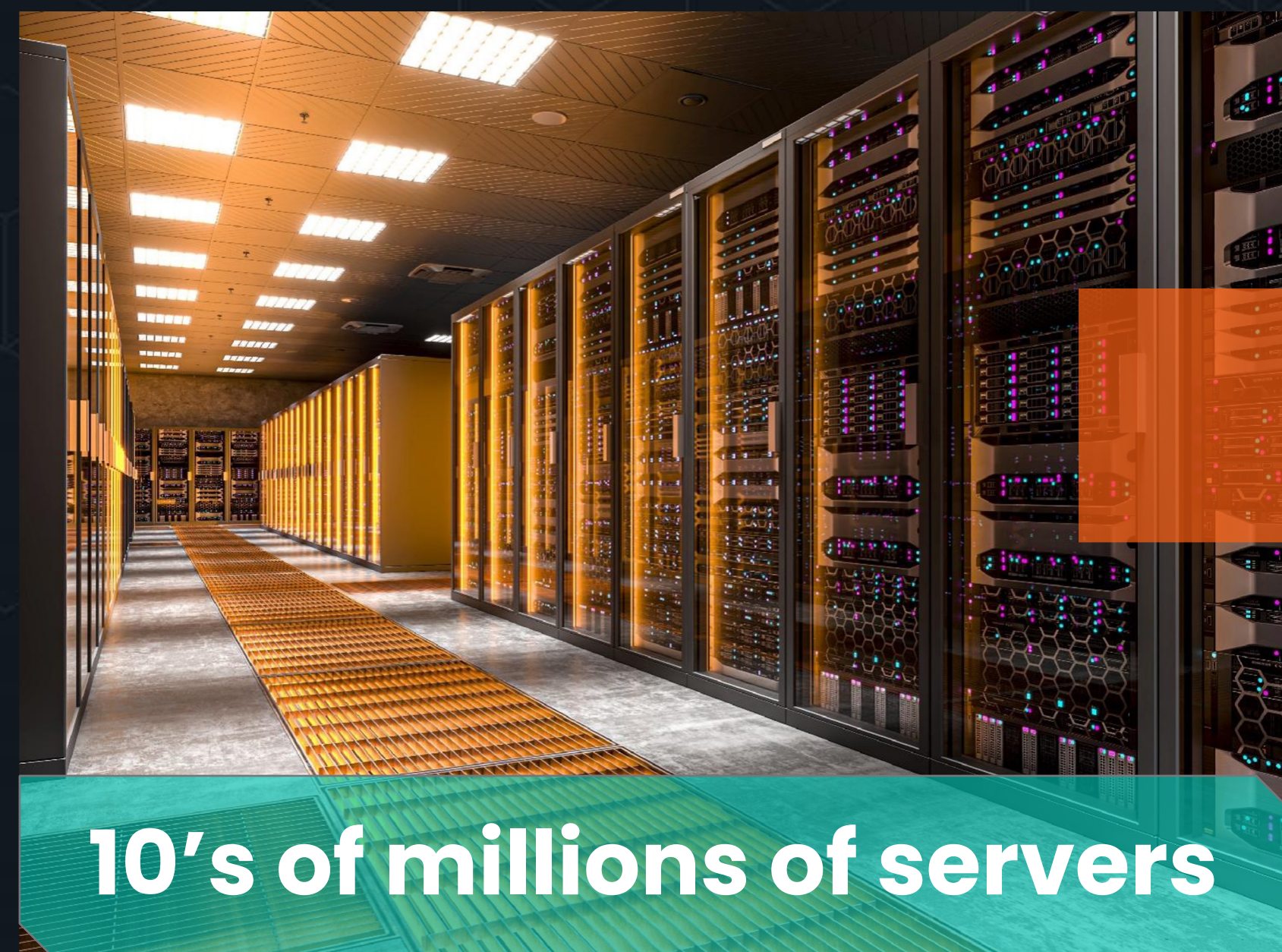
RISC-V Profile

Standard Extensions

Application Specific Chip

10's of millions of products

Decision Point: Tokens at the Edge



Physical AI is Agentic AI at the Edge

Software to Silicon for Physical AI

Sense

Data Aggregation
& Control

Think

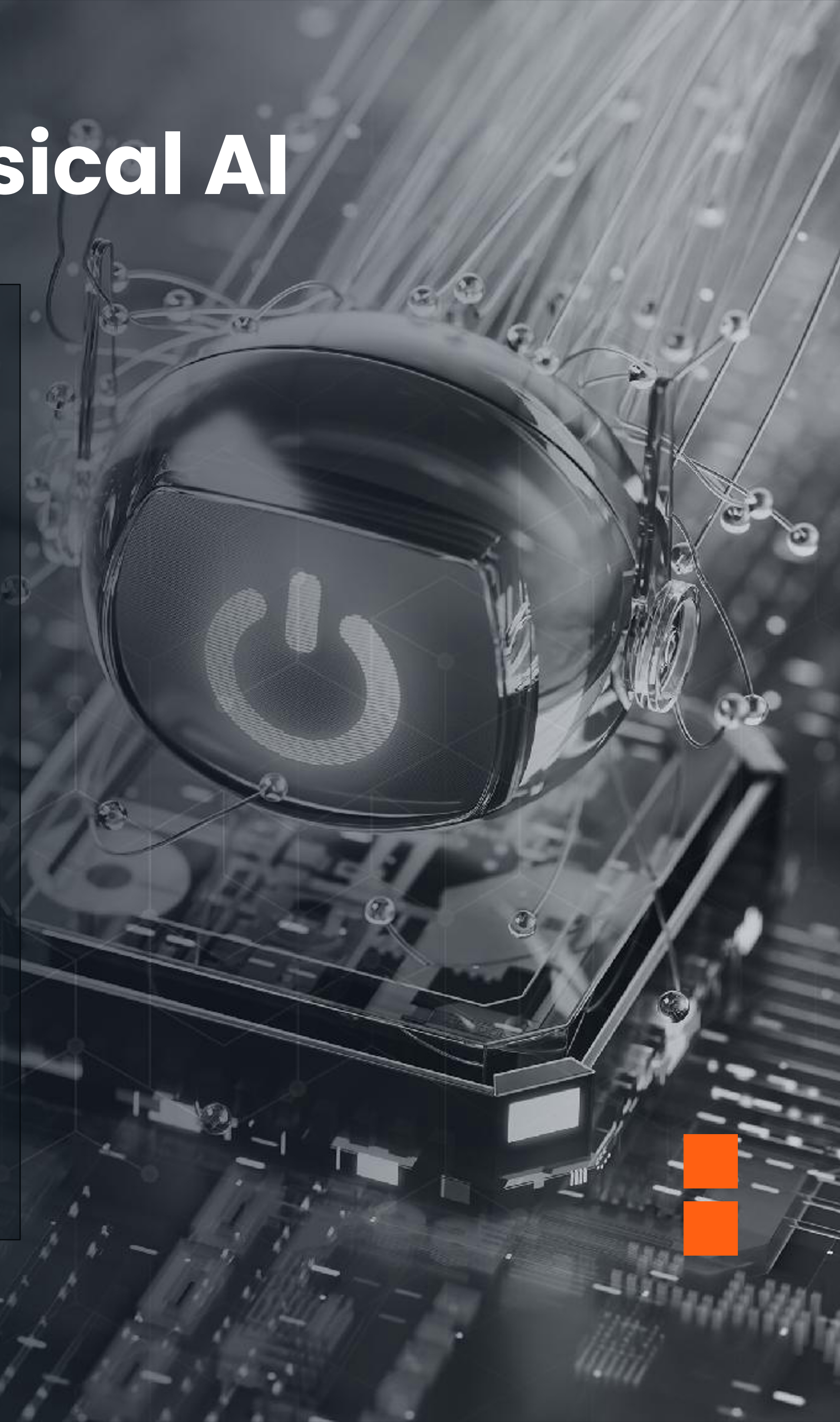
Embedded Neural
Processing Unit

Act

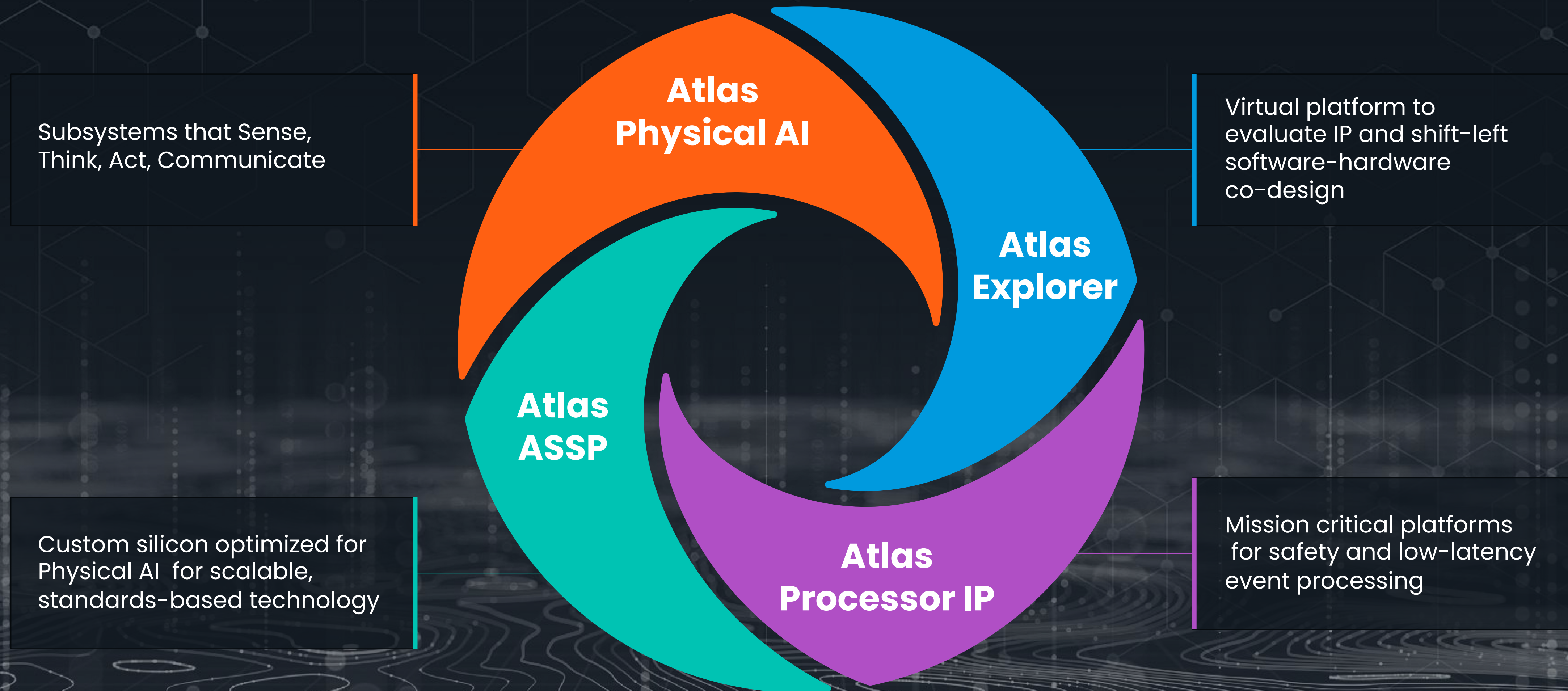
Real-Time Control & Low
Latency Event Processing

Communicate

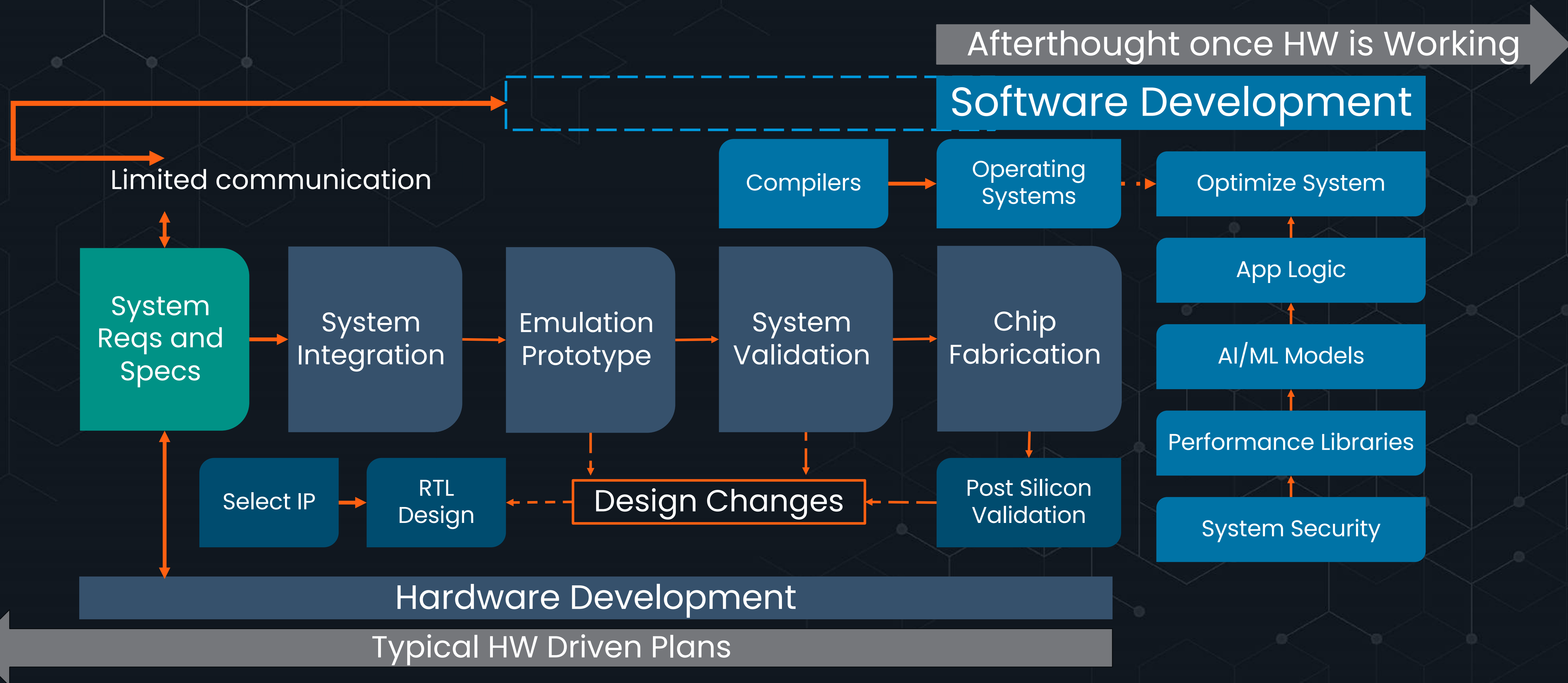
Low Latency, High Throughput
Data Orchestration



In the Agentic AI Era, Compute Needs MIPS from Software to Silicon



Typical Development Flow



Earlier Insights | Smarter Designs

Software-First Design

Atlas Explorer virtual platform for
Atlas Core Models

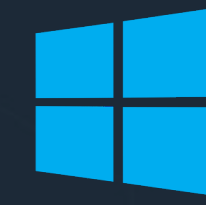
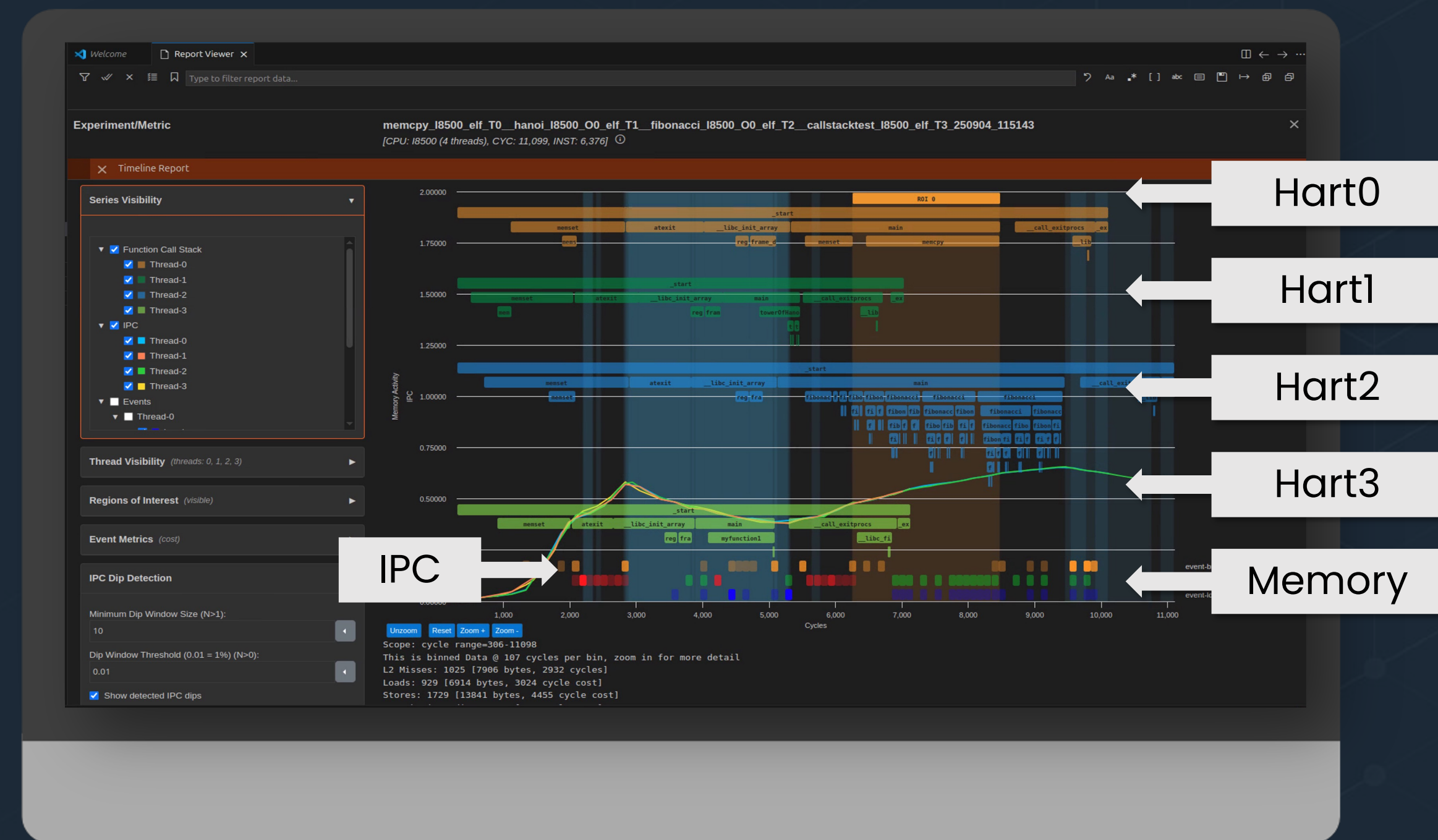
Shift-Left Development

Start your software optimization before
RTL, FPGA, and silicon availability

Platform Design Insights

Branch trends, load/store activity, ALU usage,
register pressure, cache locality, IPC & more

MIPS Atlas Explorer for Visual Studio Code

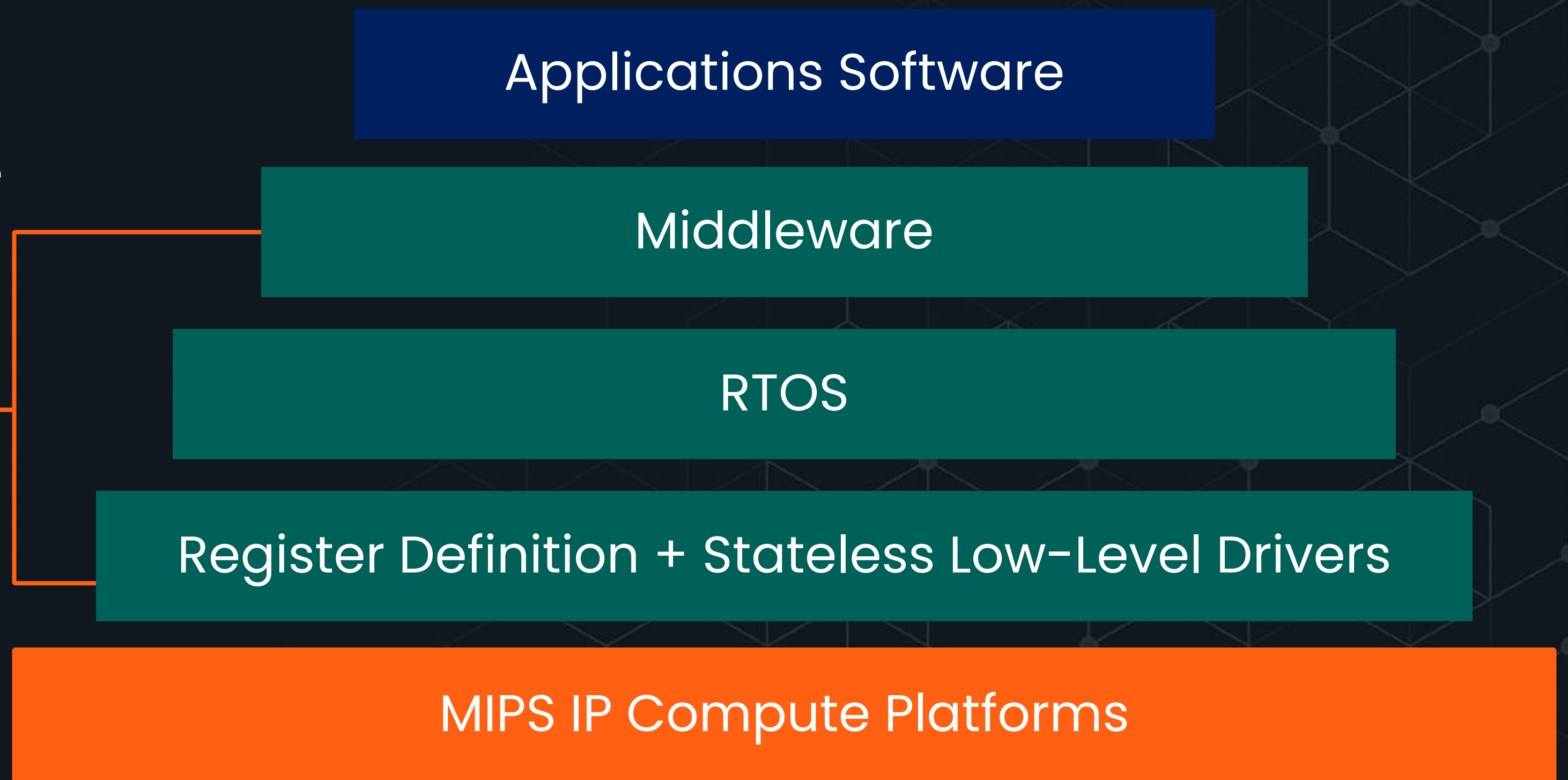


Software Migration Services

- Pre-silicon software development services
- Assist customer with architecture migrations and SDK replacements
- Customer specific LTS options available

Areas MIPS
can accelerate
development
schedules

■ Customer Software
■ Ecosystem software



"With periodic updates including CVE fixes from MIPS, our products are more secure"

- Unnamed Tier One Customer

Industry Leading AI & RISC-V Processor IP

Product Class	Atlas Processor IP Portfolio
Embedded Applications Processor	ARC RPX-100 64-bit superscalar MPU, RVA23; ASIL-B Atlas P8700 4-Wide OOO, 2-Way SMT MPU, RVA20; ASIL-B
Real-Time Linux Processor	Atlas I8500 3-Wide In-Order, 4-Way SMT MPU, RVB23
High-Performance Microcontroller	Atlas M8500 Field-Oriented Control Algorithm, 32-bit MCU, RVM23, 4-way RTMT; ASIL-B/D ARC RHX-100 32-bit MCU, RV32I + optional Vector ARC RMX-500 32-bit MCU, RV32I +optional DSP; ASIL-D
Entry Microcontroller	ARC RMX-100 32-bit MCU, RV32E / RV32I; ASIL-D
AI Acceleration / Offload	Atlas S8200 Deterministic Performance In-Order CPU host, RVA23+, SMT, RVV, RME ARC NPX6 Scalable NPU for Modern AI
Digital Signal Processing	ARC VPX Family Scalable VLIW/SIMD with vector FPU

Customer Highlight: FPGA to ASIC

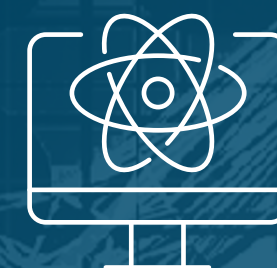


[Accelerating Chip Prototype-to-Product – HyperFRAME Research](#)

“What has stood out throughout our engagement with MIPS is how seamlessly the teams worked together to accelerate innovation.

By combining Apex’s design expertise with MIPS’ deep implementation capabilities and close alignment with GlobalFoundries, we created a highly collaborative development model that allowed us to move quickly, solve challenges in real time, and streamline the path from FPGA to ASIC.”

– **Hasan Unlu, Founder and CEO of Apex Compute**



Holistic Capabilities Accelerating Physical AI

Differentiated Value | **Embedded in the Design Cycle** | **Durable Relationships**



Deliver differentiated RISC-V CPU cores for real-time, safety, and AI segments, leveraging industry-leading multi-threaded architecture



Accelerate customer time-to-market via a robust, integrated software ecosystem



Invest in flagship custom silicon platforms powered by RISC-V IP and GF's ultra-low power nodes, optimized for latency, power, and cost

First at-scale RISC-V IP Provider from Software to Silicon

Thank You

