RISC-V SUMMIT EUROPE 2026
BOLOGNA | 8-12 JUNE, 2026 Palazzo dei Congressi

RISC-V Server Platform 1.0
One Spec to Boot Them All

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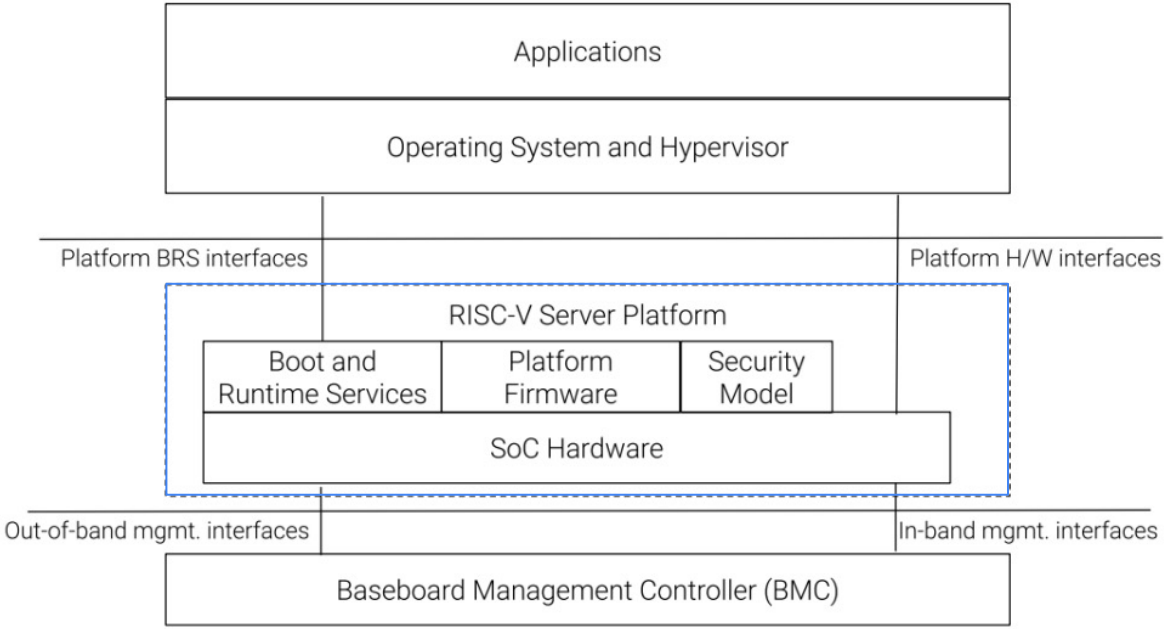
Agenda

1. Intent
2. Content
3. Task Group
4. Future

Standardized set of hardware and software capabilities



A Server Platform

- Reduce ecosystem fragmentation
- Sufficient baseline
- Seamless adoption

- Cloud & Virtualization Hosts
- Enterprise Linux Servers
- Storage, Networking & Security Appliances
- HPC & Research Clusters
- Edge / Regional Data Center

RISC-V Server Platform 1.0

RVA23S64 Profile

- Sstc, Sha, Zic64b, Zimop, V, etc.
- Sv48, Sdtrig, Sdext, Zkr, Ssccfg, Ssstrict, Ssaia
- Equivalent harts
- Minimal counter numbers, etc.

Server SoC 1.0

- Constant 1ns time
- IMSIC
- IOMMU
- PCIe 6.0
- RAS *
- QoS *
- Management *
- PCIe if assignable

Peripherals

- UART
- XHCI if USB
- AHCI if SATA
- RTC with Battery
- TPM 2.0

BRS-I 1.0

- SBI HSM
- UEFI
- ACPI
- SBI DBTR
- SBI SSE if RAS

Security Model

- RoT
- Secure Boot
- Authorization
- Updates

A joint effort of the Task Group

Alibaba Damo Academy
Andes
BOSC
Canonical
Ventana Micro Systems
AMD
Betrothed Ltd.
ByteDance
Eldorado Research Institute
Tenstorrent
Google
SUSE
Intel
SiFive
Jaguar Land Rover
Scaleway
Samsung
RISC-V International
Qualcomm
MIT
Sanechips
Rivos
Red Hat
NVIDIA

Ratified May 2026

The Future

Test specification

- OS-level tests
- Executables

Server Platform 1.1 or 2.0

- Address feedback
- Integrate Security Model
- Assess ecosystem

Virtual Server Platform

- Devices
- Migration

Meeting every first and third Monday of the month at 17:00 UTC.

https://github.com/riscv-non-isa/riscv-server-platform

https://lists.riscv.org/g/tech-server-platform