



NUCLEI

***Full-Spectrum RISC-V IP &
Automated SoC Design
from Months to Hours***

Nuclei Founder&Chairman
Bob Hu

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Who is Nuclei and Where are we from?

02

Nuclei Full-Spectrum RISC-V IP

03

Nuclei Automated SoC Design from Months to Hours

04

Summary

01

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Summary

My Personal path for RISC-V in China



- **Background (Pre-2016) :**

- EE B.S. & M.S., Shanghai Jiao Tong University
- Worked at Marvell & Synopsys, developing high-performance/low-power CPU IPs

- **2016 Vision**

- Believed China must seize the RISC-V opportunity

- **Post-2016 Actions**

- Popularized RISC-V via social media & articles
- Developed China's open-source RISC-V core: Hummingbird e203
- Authored China's first RISC-V book series

- **Founded Nuclei (June, 2018)**

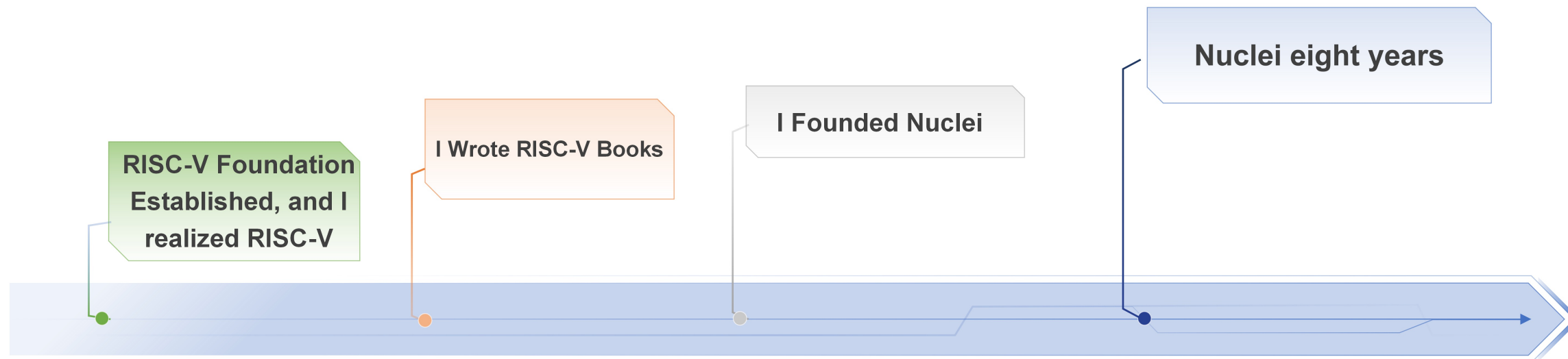
- China's first commercial RISC-V CPU IP & solutions company



Ten years in RISC-V, eight years for Nuclei



From interest to career, from one person to a venture



2015

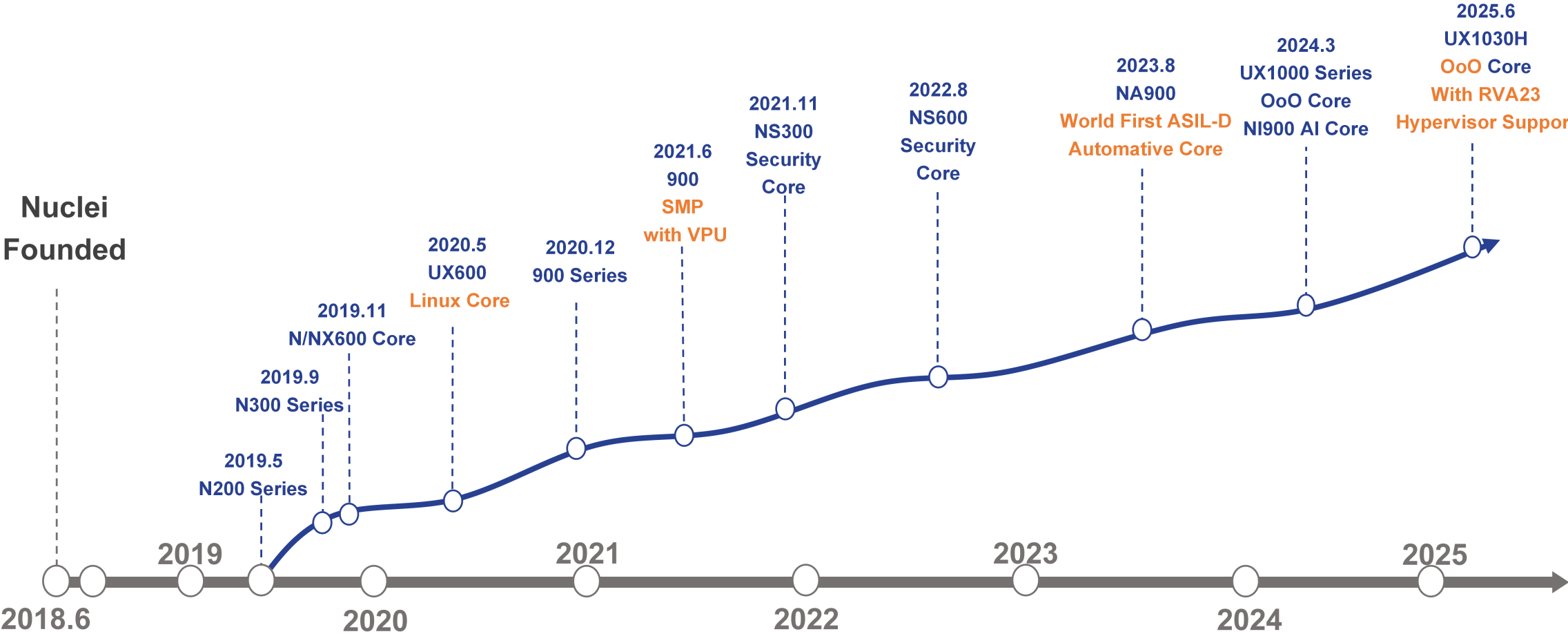
2017

2018

2026



Nuclei Delivered RISC-V IP Product Efficiently



Nuclei RISC-V IP product developed from scratch

Nuclei — Professional 3rd Party IP/Solution Vendor from China Mainland



	North America	Mainland China	Other Regions
 RISC-V			
Fabless Tech Giants	 	 	
3rd Party IP Vendors	 		
Open-Source Providers	 	 	PULP Platform
Software Toolchain		 	

01

Who is Nuclei and Where are we from?

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Nuclei Full-Spectrum RISC-V IP

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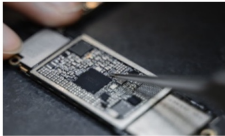
Nuclei Automated SoC Design from Months to Hours

04

Summary

RISC-V CPU IP Portfolio



General Product Line					Vertical Product Line		
	N Class 32-bit MCU, AIoT 	U Class 32-bit+MMU Linux, Edge Computing 	NX Class 64-bit Storage, AR/VR 	UX Class 64位 Arch+MMU Linux, Data Center, Network 	NS Class Security, Fintech Payment, IoT Security 	NA Class ISO26262 FUSA Automotive 	NI Class AI, ADAS, Video Communication 
1000 Series Out-of-Order 3/4/6-Wide Decode				UX1000 (SMP) Compare to ARM Cortex-A78 ARM Cortex-A76 ARM Cortex-A72/73 ARM Cortex-R82		NA1000 Compare to ARM Cortex-A78AE ARM Cortex-R82AE	NI1000
900 Series 9-Stage Pipeline Dual-Issue	N900 (SMP) Compare to ARM Cortex-R8 ARM Cortex-M7	U900 (SMP) Compare to ARM Cortex-A7	NX900 (SMP) Compare to ARM Cortex-R82 ARM Cortex-M85	UX900 (SMP) Compare to ARM Cortex-A55 ARM Cortex-A53 ARM Cortex-A35		NA900 Compare to ARM Cortex-R52+	NI900
600 Series 6-Stage Pipeline Single-Issue	N600 (SMP) Compare to ARM Cortex-R5 ARM Cortex-R4	U600 (SMP) Compare to ARM Cortex-A5	NX600 (SMP)	UX600 (SMP)	NS600		
300 Series 3-Stage Pipeline Single/Dual-Issue	N300 Compare to ARM Cortex-M33 ARM Cortex-M4F				NS300 Compare to ARM SC300	NA300	
200 Series 2-Stage Pipeline Single-Issue	N200 Compare to ARM Cortex-M3 ARM Cortex-M23						
100 Series 2-Stage Pipeline Single-Issue	N100 Compare to ARM Cortex-M0 ARM Cortex-M0+				NS100 Compare to ARM SC000		

NA - Automotive Processor



No.1 fully compliant ASIL-D automotive RISC-V CPU IP

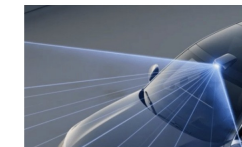
No.1 trully high-performance RISC-V CPU IP to achieve mass production in critical automotive domains

NA Series includes NA300/900/1020/1060

- NA300 compares to M33/M4/M4F
- NA900 compares to M7/R52+
- NA1020 compares to R82AE
- NA1060 compares to A78AE
- Systematic Capability: ASIL-D
- Hardware Safety Integrity: ASIL-D in DCLS mode and ASIL-B in single core or split mode
- Self-Developed STL for ASIL-B application



The most widely used RISC-V CPU IP in vehicles.



Lidar



MCU



GNSS



Radar



TSN



Switch

No.1 automotive RISC-V CPU IP with full ecosystem support includes debuggers, AUTOSAR and compilers



ETAS



CETC



VECTOR



TeraPines



OSYX



HighTec



GreenHills



IAR



LAUTERBACH



SEGGER

UX1000 — High-Performance Processor

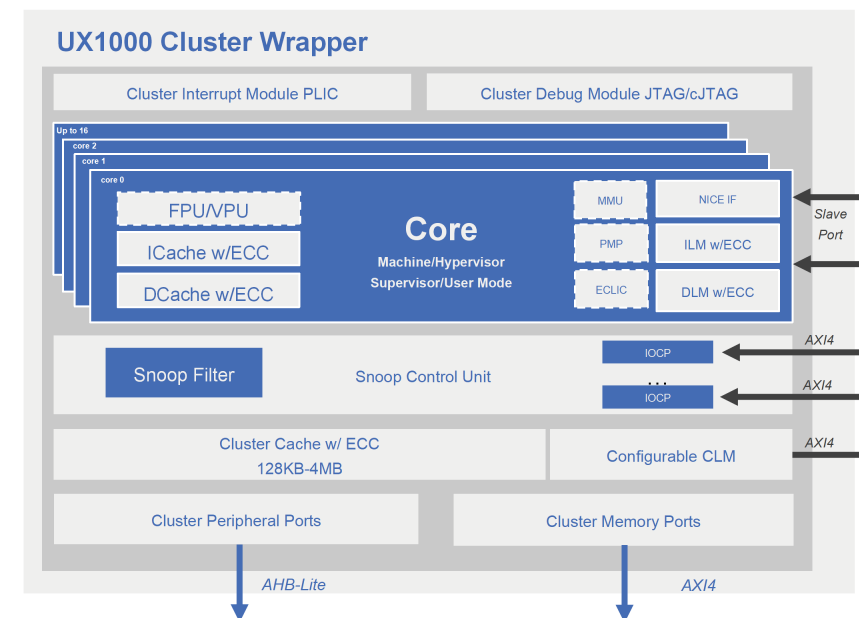


1000 series

- Pioneering **RVA23** support in the RISC-V ecosystem
- Delivering high performance with configurable OoO execution from 2 to 6 Decodes:
 - UX1020 is 2-wide decode vs. A73 or R82
 - UX1030 is 3-wide decode vs. A72
 - UX1040 is 4-wide decode vs. A76
 - UX1060 is 6-wide decode vs. A78

Cluster Features :

- | Up to 16 SMP cores in one cluster with Cache Coherency
- | Configurable IO Coherency Ports
- | Configurable Cluster Cache with SECDED ECC
- | Configurable CLM partition for deterministic data access in Cluster Cache with 128-b CLM port
- | Configurable Cluster Level Interrupt Scheme
- | Configurable Dual-Mode feature (Real-Time & Application)



Target Application



SSD



Android



ADAS



Server

Customer Massive Production Cases with Nuclei IP



GigaDevice, GD32VF103 Series MCU

1st general MCU based on RISC-V Worldwide



GigaDevice, GD32VW553 Wireless MCU

WiFi6 & BLE5.2 Dual Mode Wireless MCU based on RISC-V



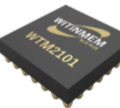
Amlogic Set-box & TV SoC

4K Smart TV Chip



Spacetouch SPV1x

AIoT Digital Audio SoC



Witintech WTM2101

1st Commercial Computing-in-Memory Chip based on RISC-V



Innochip LM620

CAT1 Chip

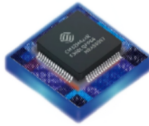
LM600

CAT1、VOLTE Chip



TIH Micro T6xx

Embedded Security Network Processor



China Mobile CM Series

China Mobile's 1st MCU, NB-IoT and Cat1 chip based on RISC-V Architecture



ASR595X

Wi-Fi 6 & BLE 5.1 Combined Solution

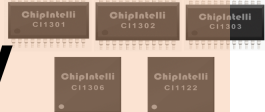
ASR1607

Location and RF Integrated Low Power Wireless Chip

ASR5861

WiFi+BT/BLE Combined SoC

350+ Customers Globally



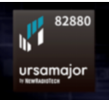
Chipintelli CI1122、CI130X

Edge AI Chip for Audio



Gejian Semi GS32F003x

Real-time Industrial Control DSP SoC



NewRadio Tech NRT82800 Series

High Performance UWB SoC



FISILINK 1030 Series

30G Ethernet Switch Chip

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Summary

Nuclei Subsys Architector: making heavy tasks “easy”



Revolutionary Cost Reduction & Accelerated Time-to-Market

Never start from scratch

All-layers subsystem configuration

Built-in consistency verifications

Full set of subsystem building blocks

AMBA compliant - multi-layer

Full set of 30+ RISC-V cores

For address mapping

Extensive library, ready-to-use

Fine-grain component configuration

Easy viewing for complex architectures

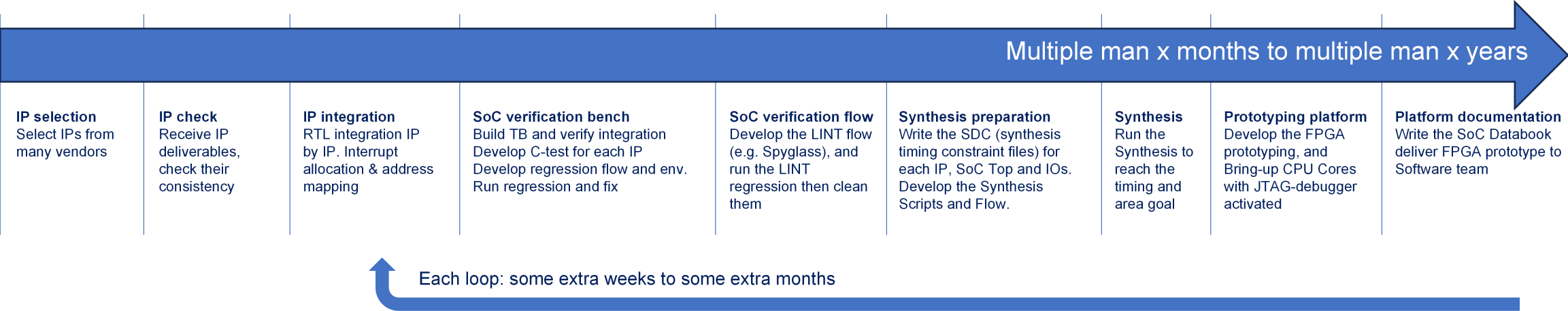
Full component configuration options

A “draw.io feel and like”

Built-in subsystem completion check

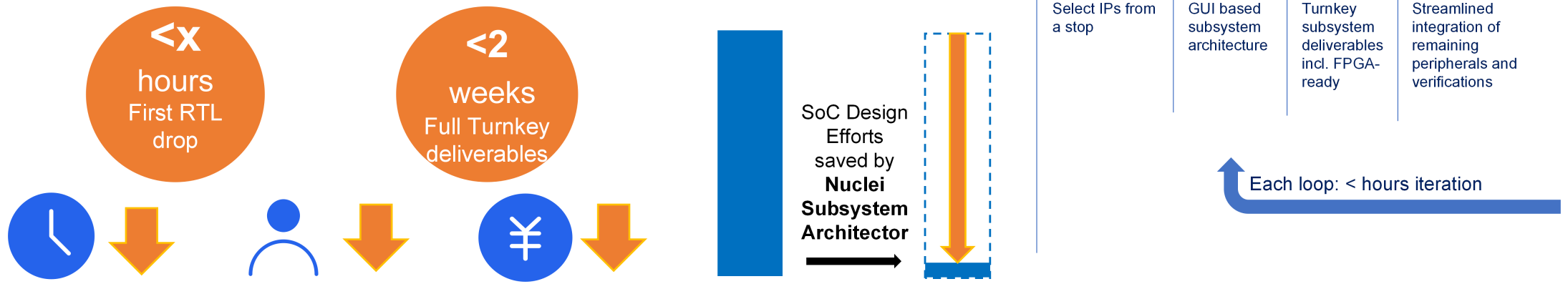
Intuitive GUI for SoC architects aims at differentiating their SoC at no design complexity costs

Traditional SoC Design vs. Nuclei Subsystem Architector



Up to 95% of logic design & verification efforts saved

Up to 95% of SDK & SW bring-up efforts saved



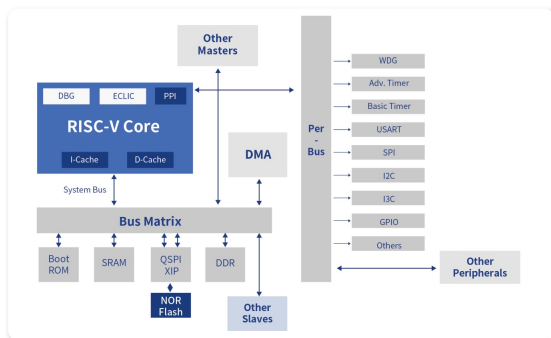


100+ turnkey processing subsystems IPs delivered



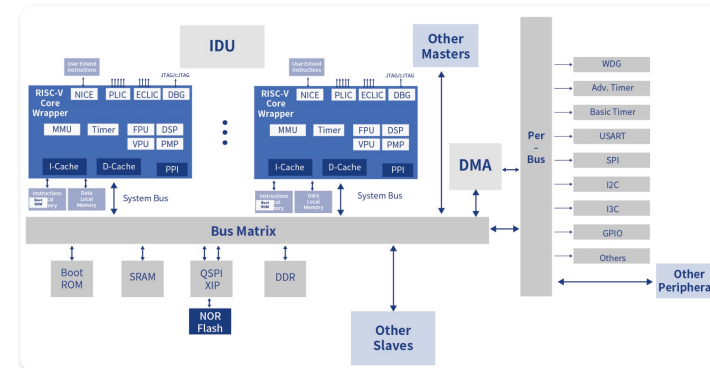
Single-core case.

Full **bring up completed by customer in 2 weeks!** after the turnkey subsystem IP delivery incl. its SDK



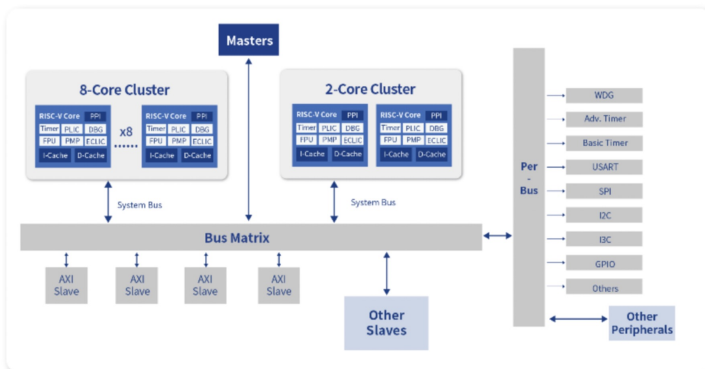
Customer Case #1: AFE+MCU

Multi-core AMP case, supports two modes (**real-time & application**), including IDU, bus matrix, etc.



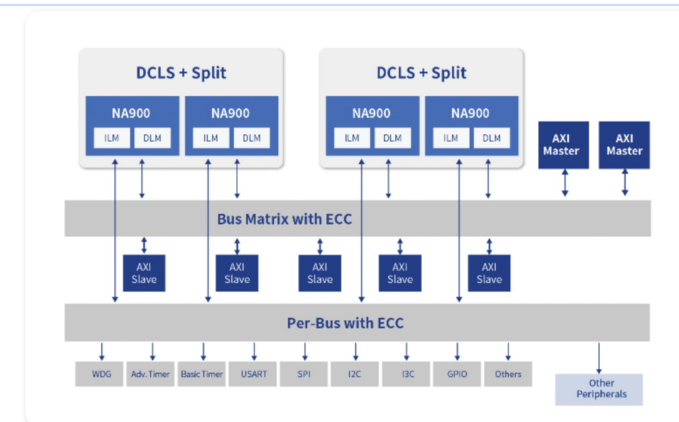
Customer Case #2: Industrial AP

Multi-core SMP case, **8-core SMP + dual-core SMP** large subsystem



Customer Case #3: Multi-core multimedia SoC

Automotive processing subsystem, relying on NA900 ASIL-D compliant multi-core. **Dual core lock step and split mode supported**



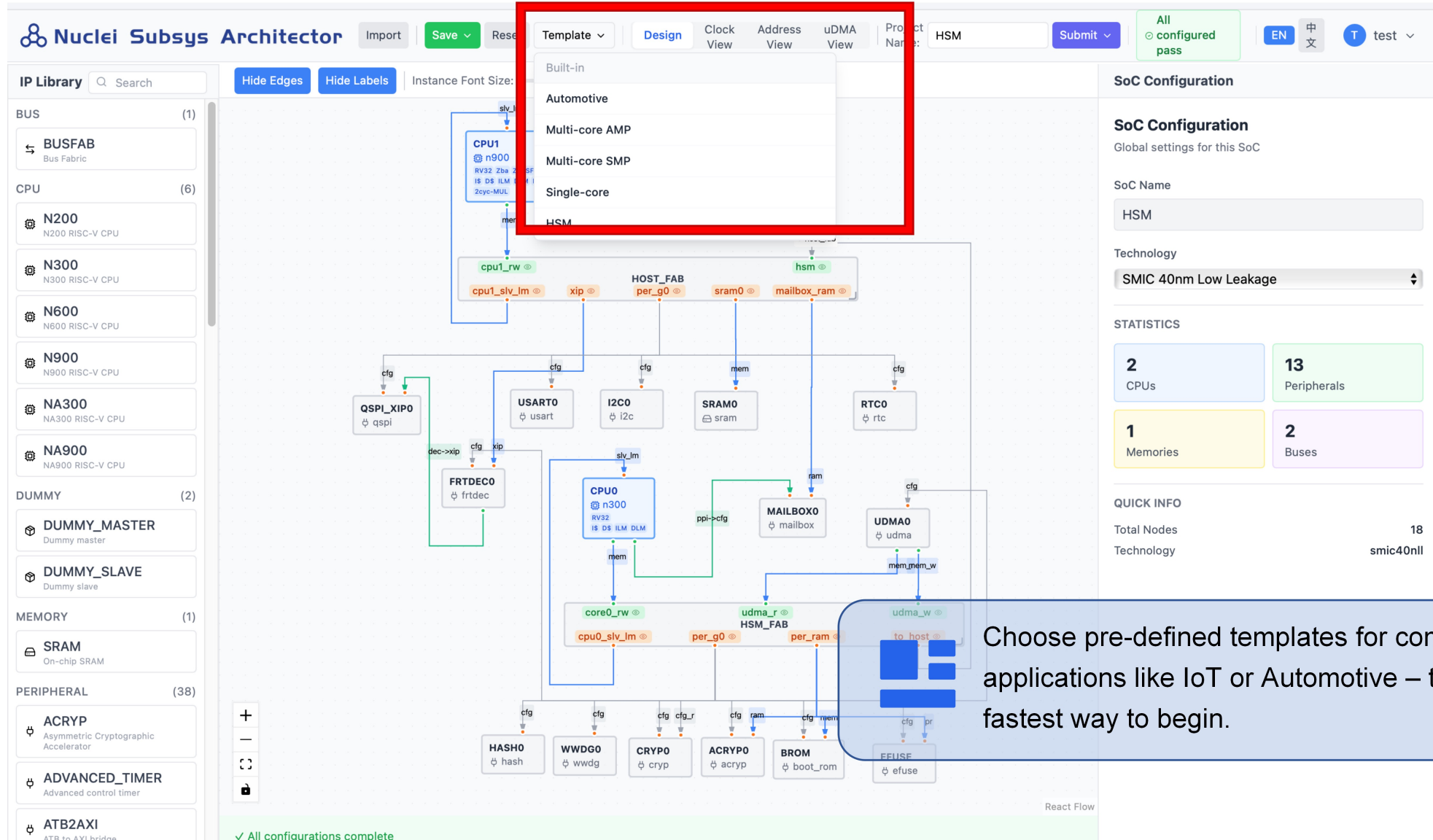
Customer Case #4: ASIL-D ZCU-like

Nuclei Subsys Architector Demo



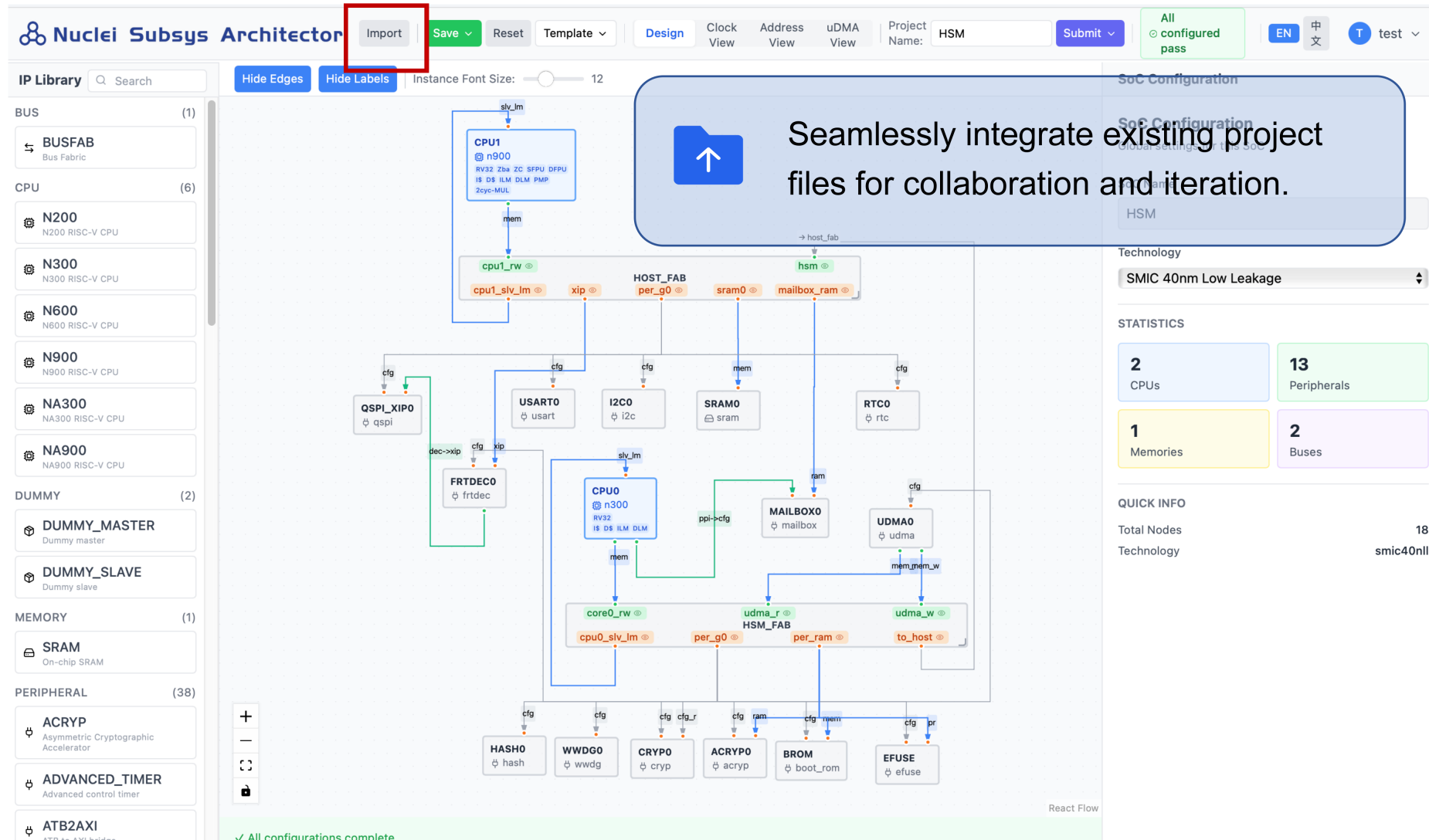
 Start with a blank canvas for complete customization and flexibility.

A SoC Design Journey (Step #1): Start from Template



The screenshot displays the Nuclei Subsys Architector interface. On the left, there is an IP Library with categories: BUS (1), CPU (6), DUMMY (2), MEMORY (1), and PERIPHERAL (38). The main workspace shows a SoC design template with components like CPU1 (n900), CPU0 (n300), HOST_FAB, and various peripherals. A red box highlights the 'Template' dropdown menu, which lists options: Built-in, Automotive, Multi-core AMP, Multi-core SMP, Single-core, and HSM. The right sidebar shows the 'SoC Configuration' panel with fields for SoC Name (HSM), Technology (SMIC 40nm Low Leakage), and statistics: 2 CPUs, 13 Peripherals, 1 Memories, and 2 Buses. A blue callout box with a plus icon contains the text: 'Choose pre-defined templates for common applications like IoT or Automotive – the fastest way to begin.'

A SoC Design Journey (Step #1): Import Project



Nuclei Subsys Architector Import Save Reset Template Design Clock View Address View uDMA View Project Name: HSM Submit All configured pass EN 中文 test

IP Library Search

BUS (1)
BUSFAB Bus Fabric

CPU (6)
N200 N200 RISC-V CPU
N300 N300 RISC-V CPU
N600 N600 RISC-V CPU
N900 N900 RISC-V CPU
NA300 NA300 RISC-V CPU
NA900 NA900 RISC-V CPU

DUMMY (2)
DUMMY_MASTER Dummy master
DUMMY_SLAVE Dummy slave

MEMORY (1)
SRAM On-chip SRAM

PERIPHERAL (38)
ACRYP Asymmetric Cryptographic Accelerator
ADVANCED_TIMER Advanced control timer
ATB2AXI ATB to AXI bridges

SoC Configuration
Global settings for this SoC
HSM

Technology
SMIC 40nm Low Leakage

STATISTICS

2 CPUs	13 Peripherals
1 Memories	2 Buses

QUICK INFO
Total Nodes 18
Technology smic40nll

Seamlessly integrate existing project files for collaboration and iteration.

React Flow

✓ All configurations complete

A SoC Design Journey (Step #2): Configure Bus

Nuclei Subsys Architector Import Save Reset Template Design Clock View Address View uDMA View Project Name: Single-core Submit All configured pass EN 中文 test

IP Library Search Hide Edges Hide Labels Instance Font Size: 12

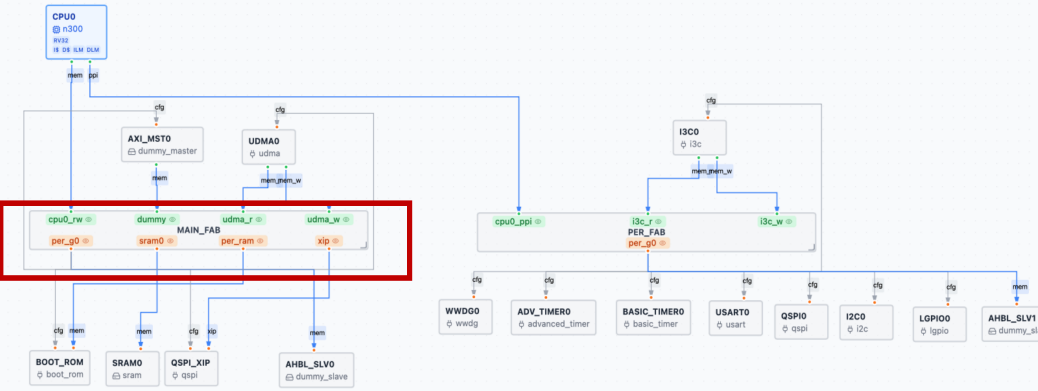
BUS (1)
BUSFAB Bus Fabric

CPU (5)
N200 N200 RISC-V CPU
N300 N300 RISC-V CPU
N600 N600 RISC-V CPU
N900 N900 RISC-V CPU
NA900 NA900 RISC-V CPU

DUMMY (2)
DUMMY_MASTER Dummy master
DUMMY_SLAVE Dummy slave

MEMORY (1)
SRAM On-chip SRAM

PERIPHERAL (38)
ACRYP Asymmetric Cryptographic Accelerator
ADVANCED_TIMER Advanced control timer
ATB2AXI ATB to AXI bridge
AXI2L2C



The diagram shows a SoC architecture with a central BUSFAB (Bus Fabric) component. It is connected to various peripherals including CPU0, AXI_MASTER, UDMA0, I3C0, WWDG0, ADV_TIMER0, BASIC_TIMER0, USART0, QSPI0, I2C0, LQPI00, and AHBL_SLV1. A red box highlights the BUSFAB and its connections to CPU0, AXI_MASTER, UDMA0, I3C0, WWDG0, ADV_TIMER0, BASIC_TIMER0, USART0, QSPI0, I2C0, LQPI00, and AHBL_SLV1.

Property Panel Delete

Instance Name
axi_mst0

Parameters
aw 16
dw 32
protocol axi

Clock Configuration
clk main_fab_clk
Type CLK_DIV
mem cpu0_cpu_clk → [object Object]
cfg cpu0_cpu_clk → [object Object]

Bus Connection Config

Port	Direction	Connection	Target
mem	master	Bus	main_fab dummy
cfg	slave	Bus	main_fab per_g0

 Define master/slave connections and set arbitration rules

✓ All configurations complete

React Flow

A SoC Design Journey (Step #2): Configure CPU IP

Nuclei Subsys Architector Import Save Reset Template Design Clock View Address View uDMA View Project Name: Automotive Submit 1 pending items EN 中文 test

IP Library Search Hide Edges Hide Labels Instance Font Size: 12

BUS (1)

- BUSFAB Bus Fabric

CPU

- N200** N200 RISC-V CPU
- N300** N300 RISC-V CPU
- N600** N600 RISC-V CPU
- N900** N900 RISC-V CPU
- NA900** NA900 RISC-V CPU

DUMMY_MASTER Dummy master

DUMMY_SLAVE Dummy slave

MEMORY (1)

- SRAM On-chip SRAM

PERIPHERAL (38)

- ACRYP Asymmetric Cryptographic Accelerator
- ADVANCED_TIMER Advanced control timer
- ATB2AXI ATB to AXI bridge
- AXI2LUCIE

Property Panel Delete

Instance Name

cpu1

Parameters

CFG_CORE_PFX nuclei900_

CPU Type Select NA900B(RV32+ASIL-B)

Internal Region Base Address(DEBUG, ECLIC, TIMER, PLIC, SMP, CIDU, etc.) 'N600_CFG_PA_SIZE'h18000

Multiplier & Divider >

Extra ISA Extension >

I/D-CACHE Cacheline Size in Byte >

Memory Protection >

DEBUG & Etrace >

Flash Bus Interface >

Local Memory(ILM/DLM) >

I/D-CACHE >

PMA >

PPI interface >

Interrupt Controller(ECLIC) >

Special Feature(ECC,NICE...) >

DSP & FPU >

VPU >

Performance/Timing Optimization >

Diagram: A system architecture diagram showing a central CPU block (CPU1) connected to various peripheral blocks. The CPU1 is connected to a MAIN_FAB block, which in turn connects to several AXI_SLAVE blocks (AXI_SLV0, AXI_SLV1, AXI_SLV2, AXI_SLV3). The CPU1 is also connected to a PER_FAB block, which connects to various peripheral blocks including WWDOG, ADV_TIMER0, BASIC_TIMER0, USART0, QSPI0, I2C0, LQSPI0, and AHB_SLV0. The diagram is enclosed in a red box.

Enable or disable standard extensions and configure all supported features

✓ All configurations complete

A SoC Design Journey (Step #2): Configure Peripherals



IP Library

Search

MEMORY (1)

SRAM

On-chip SRAM

PERIPHERAL (38)

ACRYP

Asymmetric Cryptographic Accelerator

ADVANCED_TIMER

Advanced control timer

ATB2AXI

ATB to AXI bridge

AXI2UCIE

AXI to UCIE bridge

BASIC_TIMER

Basic control timer

BOOT_ROM

Boot ROM

CRYP

Cryptographic engine using the DES, Triple-DES or AES

DBG

Debug module

DCMI

Digital Camera Interface

DDR_TOP

DDR Controller

DISP

LCD Display controller

EFUSE

Efuse

Import

Save

Reset

Template

Design

Clock View

Address View

uDMA View

Project Name: Automotive

Submit

6 pending items

EN

中文

T test

CPU0

na900

core

slave core

CPU1

na900

core

slave core

AXI_MST0

dummy_master

AXI_MST1

dummy_master

AXI_SLV0

dummy_slave

AXI_SLV1

dummy_slave

AXI_SLV2

dummy_slave

AXI_SLV3

dummy_slave

WWDG0

wwdg

ADV_TIMER0

advanced_timer

BASIC_TIMER0

basic_timer

USART0

usart

QSPI0

qspi

I2C0

i2c

GPIO0

gpio

AHB_SLV0

dummy_slave

Instance Name

wwdg0

Parameters

same_cfg

-- None --

Has secure mode

0

Clock Configuration

cfg_clk

per_fab_clk

Relation

Ratio

cfg

cpu0_cpu_clk → [object Object]

Bus Connection Config

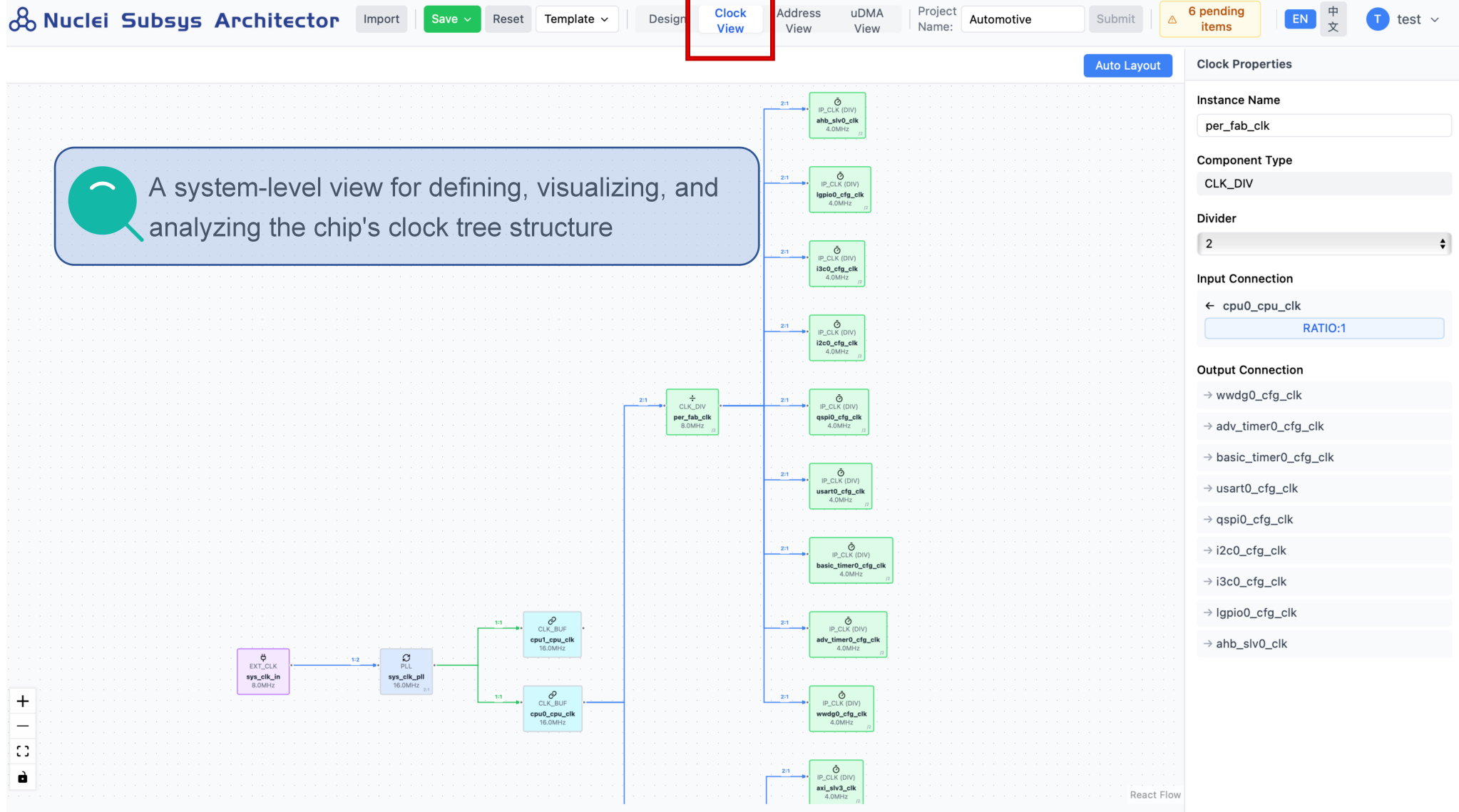
Port	Direction	Connection	Target
cfg	slave	Bus	per_fab
			per_g0

Easily configure on-chip peripherals like UART, SPI, I2C, and GPIO..

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A SoC Design Journey (Step #3): Clock View



A SoC Design Journey (Step #3): Address View



Nuclei Subsys Architector

Import

Save

Reset

Template

Design

Clock View

Address View

uDMA View

Project Name: Automotive

Submit

6 pending items

EN

中文

T test

Master Ports

12 instances

Instance	Type	Port	Dir	Connection	Group	Base Address	Def.Slv	AW	DW	LSB	Size	OID	XUSR	HAS_ECCP	Clock
axi_mst0	dummy_master	mem	M	main_fab	axi0_rw	-	-	-	32	12	-	-	-	-	ratio
axi_mst1	dummy_master	mem	M	main_fab	axi1_rw	-	-	-	32	12	-	-	-	-	ratio
cpu0	na900	mem	M	main_fab	cpu0_rw	-	-	-	-	12	-	-	-	-	ratio_rev
cpu0	na900	slave_mem	M	main_fab	cpu0_slave_rw	-	-	-	-	12	-	-	-	-	ratio_rev
cpu1	na900	mem	M	main_fab	cpu1_rw	-	-	-	-	12	-	-	-	-	ratio_rev
cpu1	na900	slave_mem	M	main_fab	cpu1_slave_rw	-	-	-	-	12	-	-	-	-	ratio_rev
cpu0	na900	ppi	M	per_fab	cpu0_ppi	-	-	-	-	12	-	-	-	-	ratio_rev
cpu0	na900	slave_ppi	M	per_fab	cpu0_slave_ppi	-	-	-	-	12	-	-	-	-	ratio_rev
cpu1	na900	slave_ppi	M	per_fab	cpu1_slave_ppi	-	-	-	-	12	-	-	-	-	ratio_rev
cpu1	na900	ppi	M	per_fab	cpu1ppi	-	-	-	-	12	-	-	-	-	ratio_rev
i3c0	i3c	mem_r	M	per_fab	i3c_r	-	-	32	-	32	-	-	-	-	ratio
i3c0	i3c	mem_w	M	per_fab	i3c_w	-	-	32	-	32	-	-	-	-	ratio

Slave Ports

15 instances

Instance	Type	Port	Dir	Connection	Group	Base Address	Def.Slv	AW	DW	LSB	Size	OID	XUSR	HAS_ECCP	Clock
axi_slv1	dummy_slave	mem	S	main_fab	axi_g0	0x1000_0000	☐	16	32	16	64KB	-	-	-	ratio
axi_slv0	dummy_slave	mem	S	main_fab	axi_g0	0x1001_0000	☐	16	32	16	64KB	-	-	-	ratio
axi_slv2	dummy_slave	mem	S	main_fab	axi_g1	0x1100_0000	☐	16	32	16	64KB	-	-	-	ratio
axi_slv3	dummy_slave	mem	S	main_fab	axi_g1	0x1101_0000	☐	16	32	16	64KB	-	-	-	ratio
wwdg0	wwdg	cfg	S	per_fab	per_g0	0x0400_0000	☐	-	-	12	4KB	-	-	-	ratio
adv_timer0	advanced_timer	cfg	S	per_fab	per_g0	0x0400_1000	☐	-	-	12	4KB	-	-	-	ratio
basic_timer0	basic_timer	cfg	S	per_fab	per_g0	0x0400_2000	☐	-	-	12	4KB	-	-	-	ratio
usart0	usart	cfg	S	per_fab	per_g0	0x0400_3000	☐	-	-	12	4KB	-	-	-	ratio
qspi0	qspi	cfg	S	per_fab	per_g0	0x0400_4000	☐	-	-	12	4KB	-	-	-	ratio

= Reset to auto

A centralized view for managing and visualizing the entire SoC address space allocation, ensuring a holistic overview of memory mapping.

A SoC Design Journey (Step #3): uDMA View



Nuclei Subsys Architector

Import

Save

Reset

Template

Design

Clock View

Address View

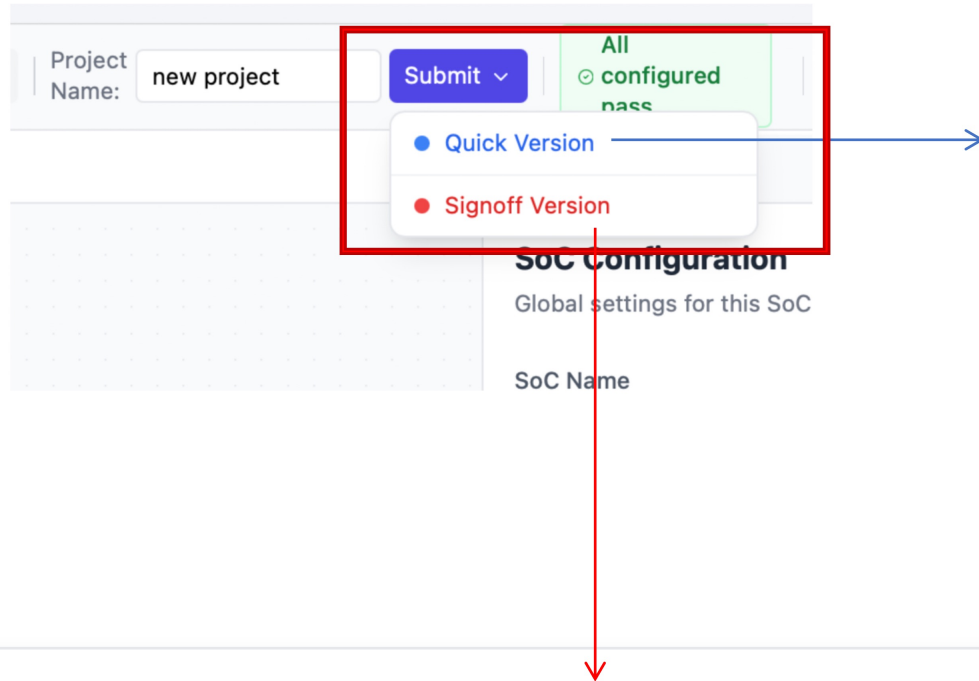
uDMA View

Proj Nan

Instance	Type	Signal	uDMA	Channel	Bit	Connection	uDMA Matrix View
adv_timer0	advanced_timer	COM	-- UDMA --	-- Ch -	-	-	
adv_timer0	advanced_timer	TRG	-- UDMA --	-- Ch -	-	-	
adv_timer0	advanced_timer	UEV	-- UDMA --	-- Ch -	-	-	
adv_timer0	advanced_timer	CC1	-- UDMA --	-- Ch -	-	-	
adv_timer0	advanced_timer	CC2	-- UDMA --	-- Ch -	-	-	
adv_timer0	advanced_timer	CC3	-- UDMA --	-- Ch -	-	-	
adv_timer0	advanced_timer	CC4	-- UDMA --	-- Ch -	-	-	
basic_timer0	basic_timer	REQ	-- UDMA --	-- Ch -	-	-	
usart0	usart	TX	-- UDMA --	-- Ch -	-	-	
usart0	usart	RX	-- UDMA --	-- Ch -	-	-	
qspi0	qspi	TX	-- UDMA --	-- Ch -	-	-	
qspi0	qspi	RX	-- UDMA --	-- Ch -	-	-	
i2c0	i2c	TX	-- UDMA --	-- Ch -	-	-	
i2c0	i2c	RX	-- UDMA --	-- Ch -	-	-	

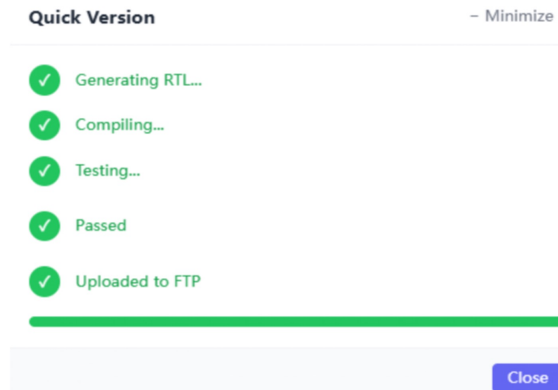
A dedicated view for defining, configuring, and analyzing DMA channel assignments and data transfer paths

A SoC Design Journey (Step #4): Submission



Quick Version(**within hours**)

A streamlined, automated check to verify your configured subsystem for fast iteration and corrections early in your design cycle.



Signoff Version (**withinin two weeks**)

Triggers the full generation flow to produce a production-ready, silicon-proven design package.

- Subsystem Database & Fully Assembled, Synthesizable RTL
- Comprehensive Test Cases & Non-Regression Test Suite
- SDC Timing Constraints & Synthesis Reference Scripts
- Software Package: Drivers + SDK + Ctest + App Demo

01

Who is Nuclei and Where are we from?

02

Nuclei Full-Spectrum RISC-V IP

03

Nuclei Automated SoC Design from Months to Hours

04

Summary

- | | | | |
|---|---------|--|--------------------|
|  | 5G Comm |  | Industrial Control |
|  | AI |  | Automotive |
|  | IoT |  | Storage |
|  | MCU |  | Networking |

-
- The diagram shows the NUCLEI logo at the center, which consists of a stylized icon of three interconnected circles followed by the word "NUCLEI" in a bold, sans-serif font. Surrounding the logo is a circular dashed line. Three solid blue triangles are positioned at the top, bottom-left, and bottom-right of this circle. Outside the dashed circle, there are three rounded rectangular boxes: one at the top containing "~120 Employees", one at the bottom-left containing "&D", and one at the bottom-right containing "5 Sites".

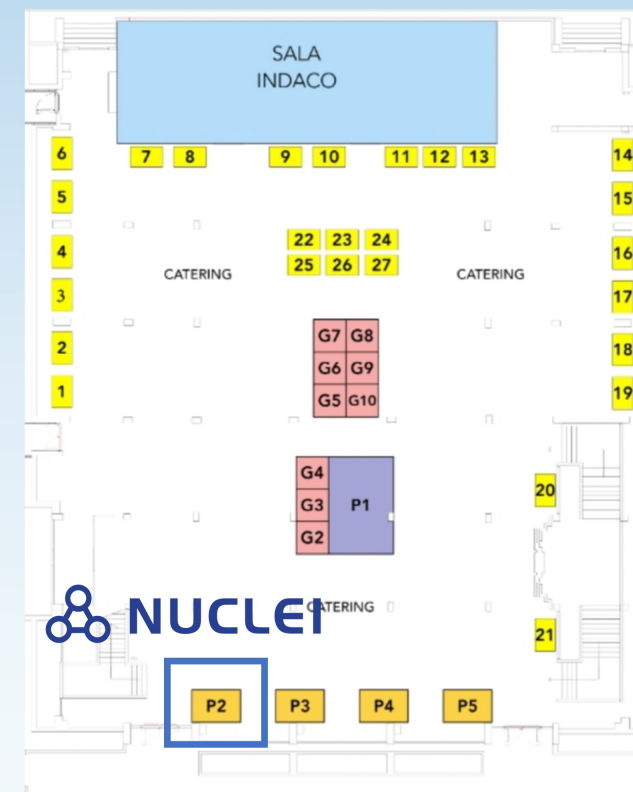
- The diagram consists of six rounded rectangular boxes arranged in a 3x2 grid. Each box contains an icon on the left and a text label on the right. The icons are: a list with a minus sign, a server rack, a shield with a checkmark, three arrows pointing right, a warning triangle, and a double-headed arrow. The text labels are: 'Rich Configurations', 'Robust Coding Format', 'Info Security Solutions', 'Scalable Extensions', 'Functional Safety Solution', and 'Flexible Business Model & Customer Support'.

	Rich Configurations
	Robust Coding Format
	Info Security Solutions
	Scalable Extensions
	Functional Safety Solution
	Flexible Business Model & Customer Support

-
- A hexagonal grid pattern featuring logos of various Chinese semiconductor companies. The logos are arranged in a honeycomb-like structure, with some hexagons being light blue and others white. The companies represented include:
- CAITERAH** (加特兰)
 - 通创集成电路**
 - 芯联集成**
 - 安路科技** (AN LOGIC)
 - 晶晨半导体** (Amlogic)
 - ASR MICROELECTRONICS** (翱捷)
 - 速显微** (THORSEMI)
 - GigaDevice** (兆易创新)
 - 中国移动** (China Mobile)
 - 纽瑞芯科技** (NEURADIODTEC)
 - 方寸微电子** (FANG CUN MICROELECTRONICS)
 - VeriSilicon** (芯原)
 - FISILINK** (飞思灵)
 - AISTARTEK** (智芯科)
 - WITINMEM** (慧存科技)
 - ChipIntelli** (启英泰伦)
 - 裕太微电子**
 - GeoforceChip** (傲世芯片)
 - BinarySemi** (二进制)
 - SILERGY** (矽力杰)
 - 西南集成**
 - CHIPWAYS** (琪埔维)
 - JOUlwATT** (杰华特)



welcome to our booth



Thank You!