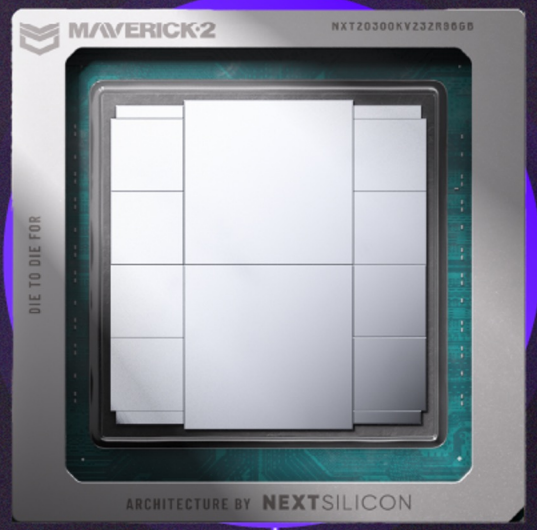
Yiftach Gilad
VP OF CPU

RISC-V SUMMIT EUROPE 2026

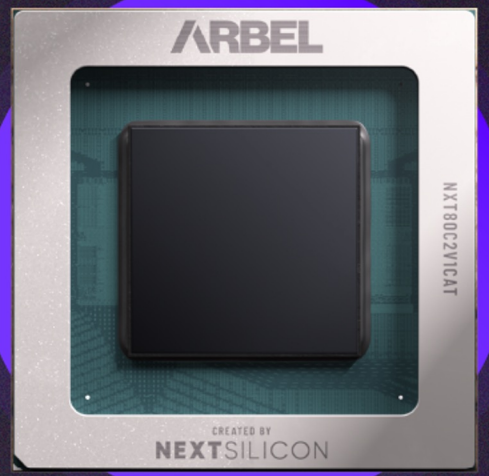
NEXTSILICON

ALWAYS IN PURSUIT OF A BETTER WAY TO COMPUTE.

MAVERICK
ACCELERATOR



MAVERICK·2
ACCELERATOR



ARBEL
RISC-V CPU

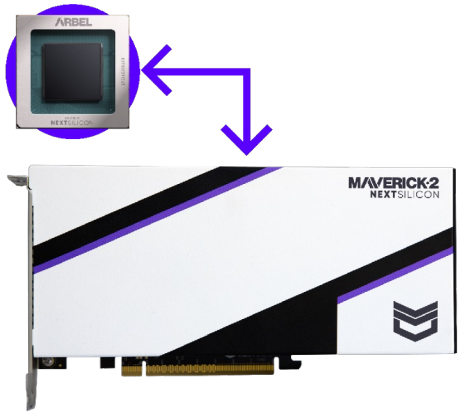
WHY RISC IT?

3 AMBITIOUS GOALS

A **server-class** general-purpose high performance RISC-V CPU

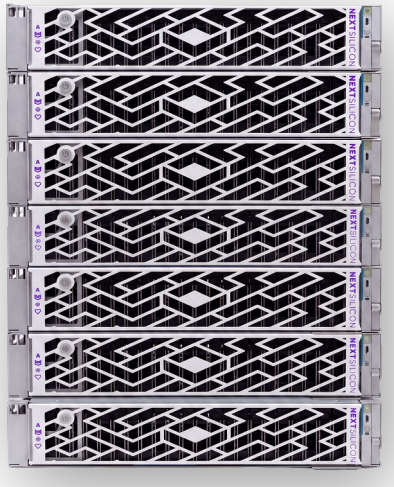
GOAL 01

High performance RISC-V CPU host & assist for Maverick



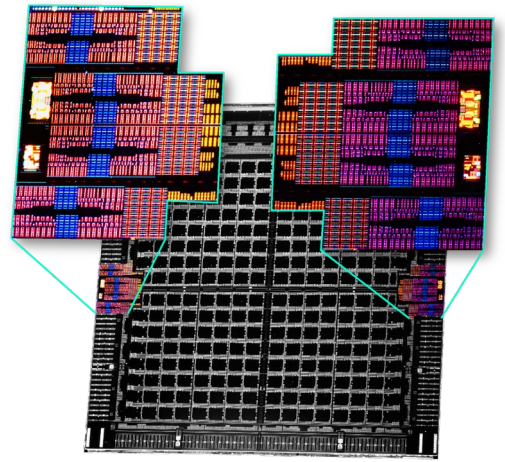
GOAL 02

Standalone RISC-V CPU server for AI



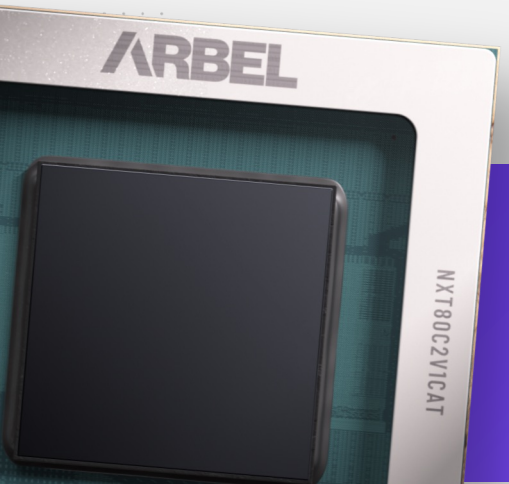
GOAL 03

Efficient core clusters to be integrated on the Maverick chip

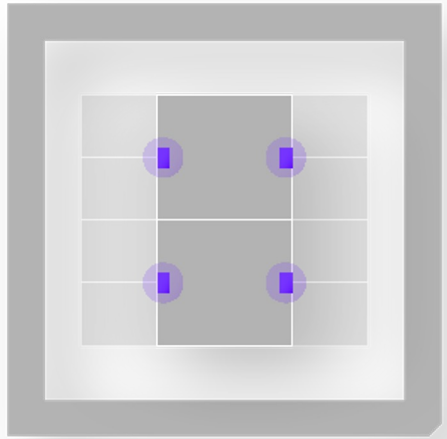


ARBEL PROGRAM EXISTING SOLUTIONS

Best-in-class
performance RISC-V CPU

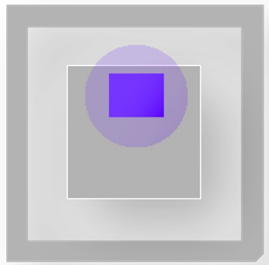


Q2'24



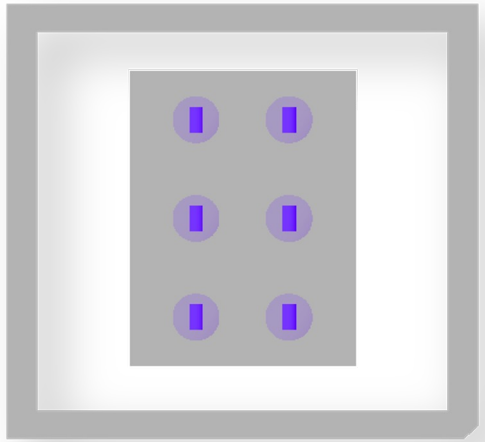
- **Integrated with accelerator**
- **Single-core 1GHz**
- **POC for OOO superscalar core**

Q1'26



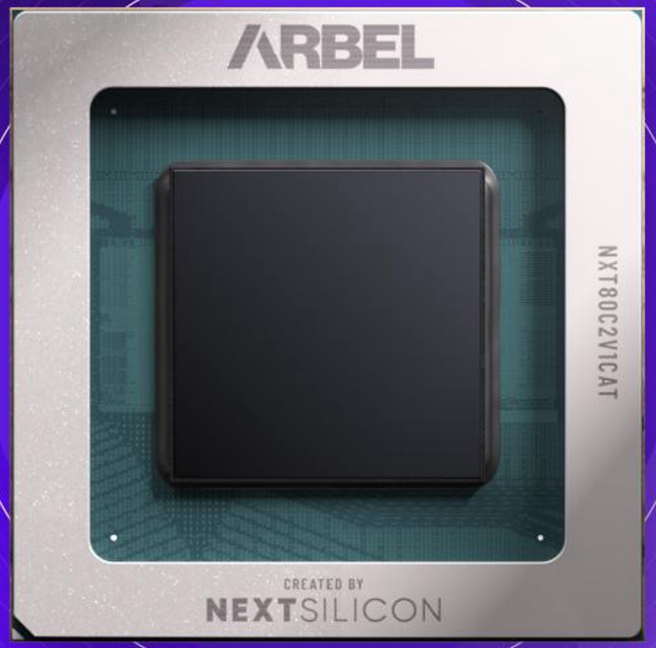
- **Test chip**
- **P-core 2nd gen**
- **Dual-core system**
  2.4GHz

PRE-SILICON



- **Integrated with accelerator**
- **multi core coherency**
- **Additional ISA**
- **Design is completed**

ARBEL TC



RISC-V CPU TEST CHIP
BY NEXTSILICON

LIVE DEMO AT BOOTH P3

RISC-V SUMMIT EUROPE 2026

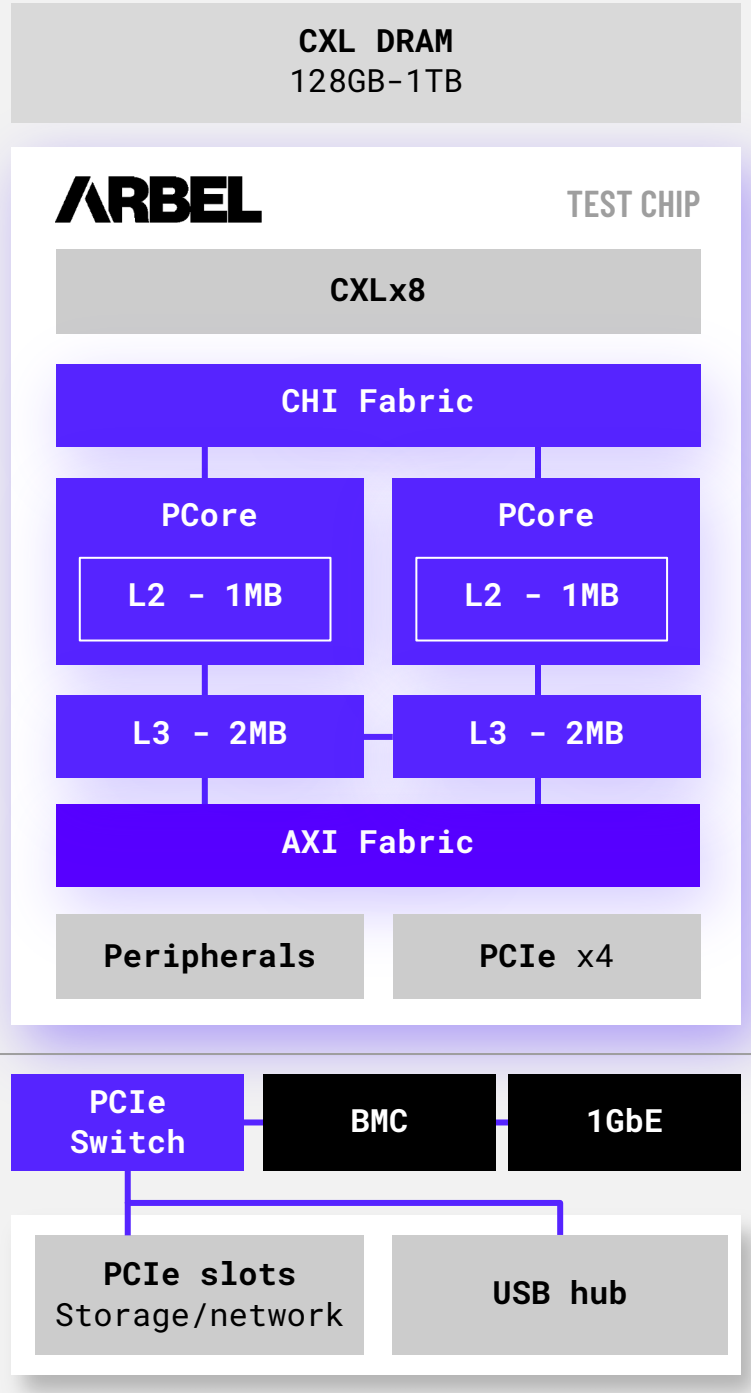
ARBEL TEST CHIP EVALUATION BOARD

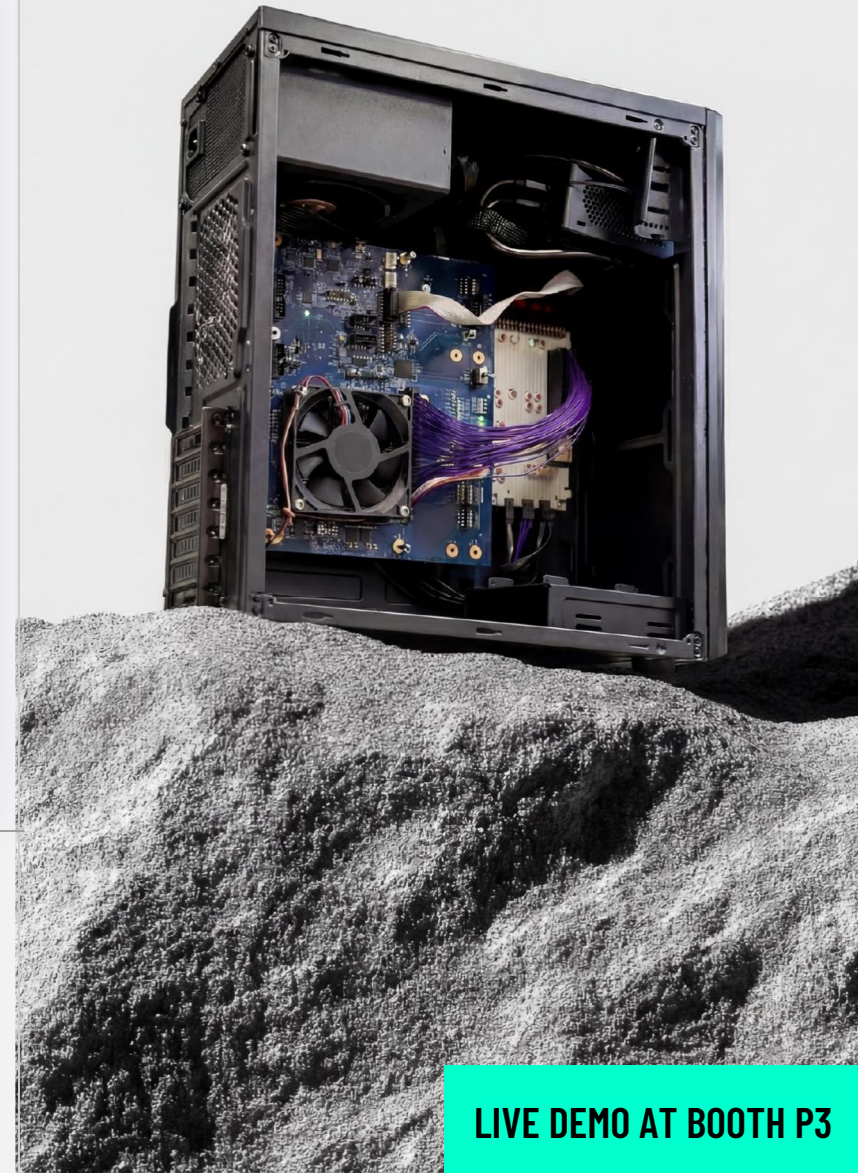
System Configuration

- **Dual Core** Full Coherency
- **PCIe:** PCIe Gen5 x4
- **DRAM:** CXL x8 DRAM up to 256GB
- **Peripherals:**
  - PCIe Switch (USB, network)
  - Network card
  - NVMe

Program Status

- **System is functional** at customer
- **Dual Core Yocto Linux & Ubuntu** Up & Running
- Toolchain support - **GCC15 and LLVM**
- **Benchmarks performance - Great silicon performance** with full correlation to simulator





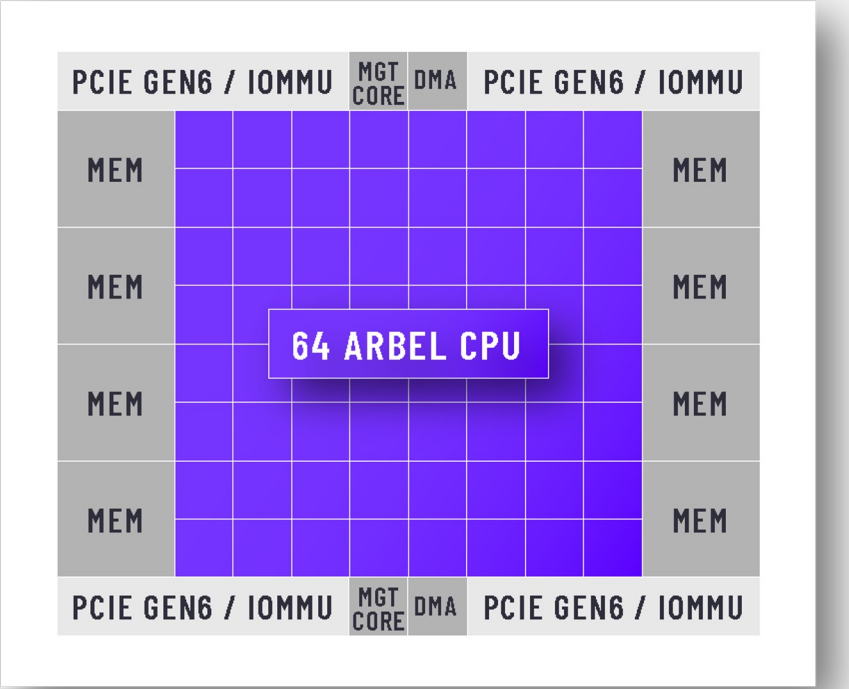
LIVE DEMO AT BOOTH P3


ARBEL
NXT80C2V1CAT
CREATED BY
RISC-V // SERVER CLASS CPU //
ARBEL
THE BEST RISC-V. PERIOD.
NEXTSILICON

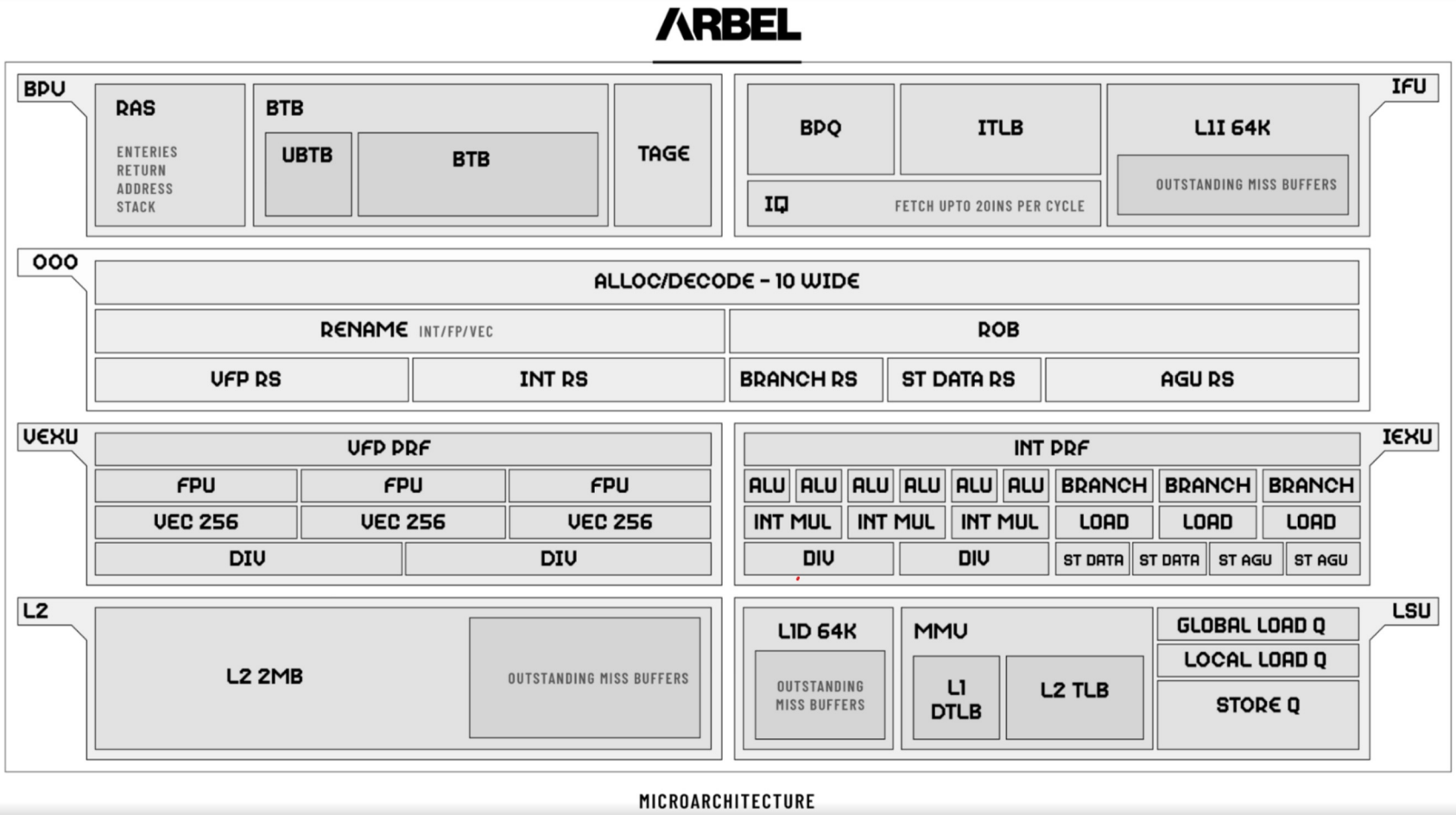
ARBEL SPECIFICATION

Application cores + NOC	64 cores - 64KB, 2MB, 2MB+ L1/L2/L3 cache size per core CHI based coherent NOC
CPU Core Frequency	~3.4 GHz
DRAM/IO Technology	DDR5 or LPDDR6/ PCIe GEN6
Core ISA	RVA23+ Mandatory + some optional extensions + low precision
Vectorization	3X256 bit
Virtualization	H extension + IO MMU
Server grade	SOC & server spec compliance ; reliability. security & debuggability
Power	250W TDP

ARBEL BLOCK DIAGRAM



ARBEL RISC-V PCORE



MICROARCHITECTURE

- **Top class Branch Predictors**
  - RAS, UBTB, BTB, tage and itage
  - 128B branch prediction width
- **Wide machine:**
  - High fetch BW - 20 inst/cyc
  - High allocation BW - 10 inst/cyc
  - 16 parallel scalar execution - ALUs/AGUs/STDs/Branch
  - 4 Loads & 2 stores
  - High retirement BW
- **High caching capacity:**
  - L1 I/D caches (64KB), L2 cache (2MB)
  - L1 I/D TLBs, L2-TLB (4K); PWC
- **Short execution latency:**
  - 1 cycle ALU to use latency
  - 4 cycle load to use latency
- **prefetchers and predictors**
  - L2 & L3 prefetchers
  - L1 stride prefetcher
  - more..
- **strong FP and vector unit**
  - **3X256 vector**

ARBEL PERFORMANCE LEADERSHIP

2.6
NextSilicon-derived
SPECint2017®/GHz(est.)

3.4
NextSilicon-derived
SPECfp2017®/GHz(est.)

The Arbel CPU will be a performance leader

- **Benchmarks** - stream, coremark, coremark-pro, hpcg, gups, NAS, spec-cpu
- **Accurate simulator modeling** - proven correlation to FPGA and silicon
- **Test chip simulations** - No compiler optimizations, Little performance tuning, Scalar only (vectorization is not modeled for spec-cpu)
- **Arbel CPU -**
  - performance features modeling and bottleneck analysis is ongoing
  - Compiler optimizations work to be upstreamed

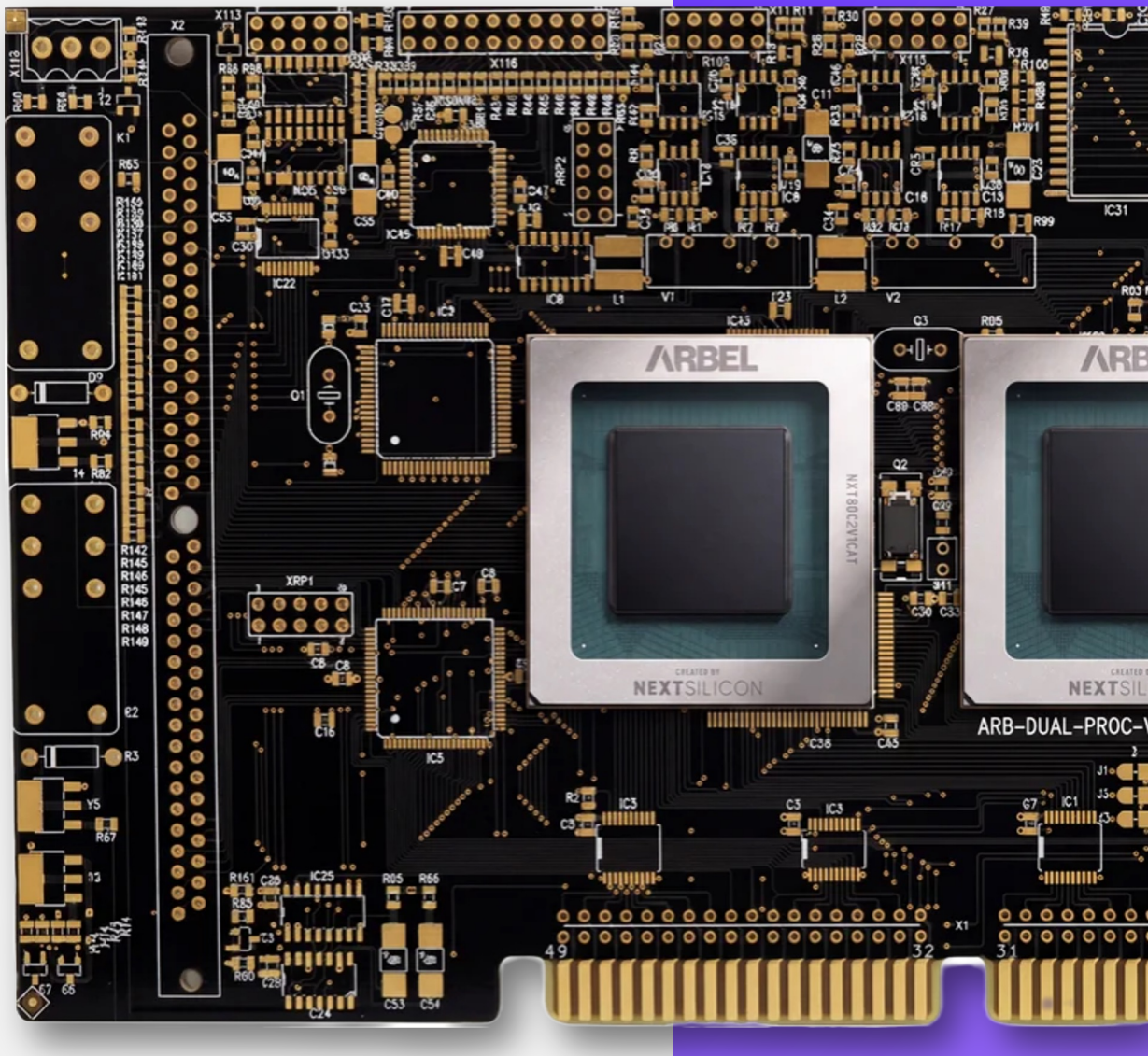
	ARBEL		
Benchmark	**Test Chip simulation**	**Arbel 64 cores target**	**Industry Leaders**
NextSilicon-derived SPECint2017® / GHz (est.)	1.93*	**2.6** est.	2.3 est.
NextSilicon-derived SPECfp2017® / GHz (est.)	2.53*	**3.4** est.	2.9 est.

SPEC CPU® 2017 is a retired benchmark. SPEC is no longer reviewing or publishing new results for this benchmark. See www.spec.org/cpu2017 for more information. Competitor figures are NextSilicon internal estimates modeled using cycle-level simulation and publicly available performance data as of May 2026. All Arbel and competitor figures are estimates and have not been reviewed or endorsed by SPEC or any third party. Actual competitor performance may differ. SPEC® is a registered trademark of the Standard Performance Evaluation Corporation. SPECint® and SPECfp® are registered trademarks of SPEC.

DUAL CHIP COHERENT SYSTEM

Scalable 128-core performance

- **128 Coherent RISC-V Cores:** Two Arbel V4 dies interconnected via repurposed PCIe Gen6 interfaces.
- **Chip to Chip communication:** Proprietary CHI based protocol over PCIe x16 provides SoC-fabric class chip to chip connectivity.
- **Unified Memory Space:** Fully coherent access across all memory and peripherals of both chips.



Conceptual OCP-HPM Coherent Dual-Chip Arrangement

ARBEL BY NEXTSILICON

TAKING RISC-V TO THE SERVER WORLD

THANK YOU.

VISIT US AT BOOTH P3