Ultra Low Power RISC-V Core
Retention with Warm Restart Extension

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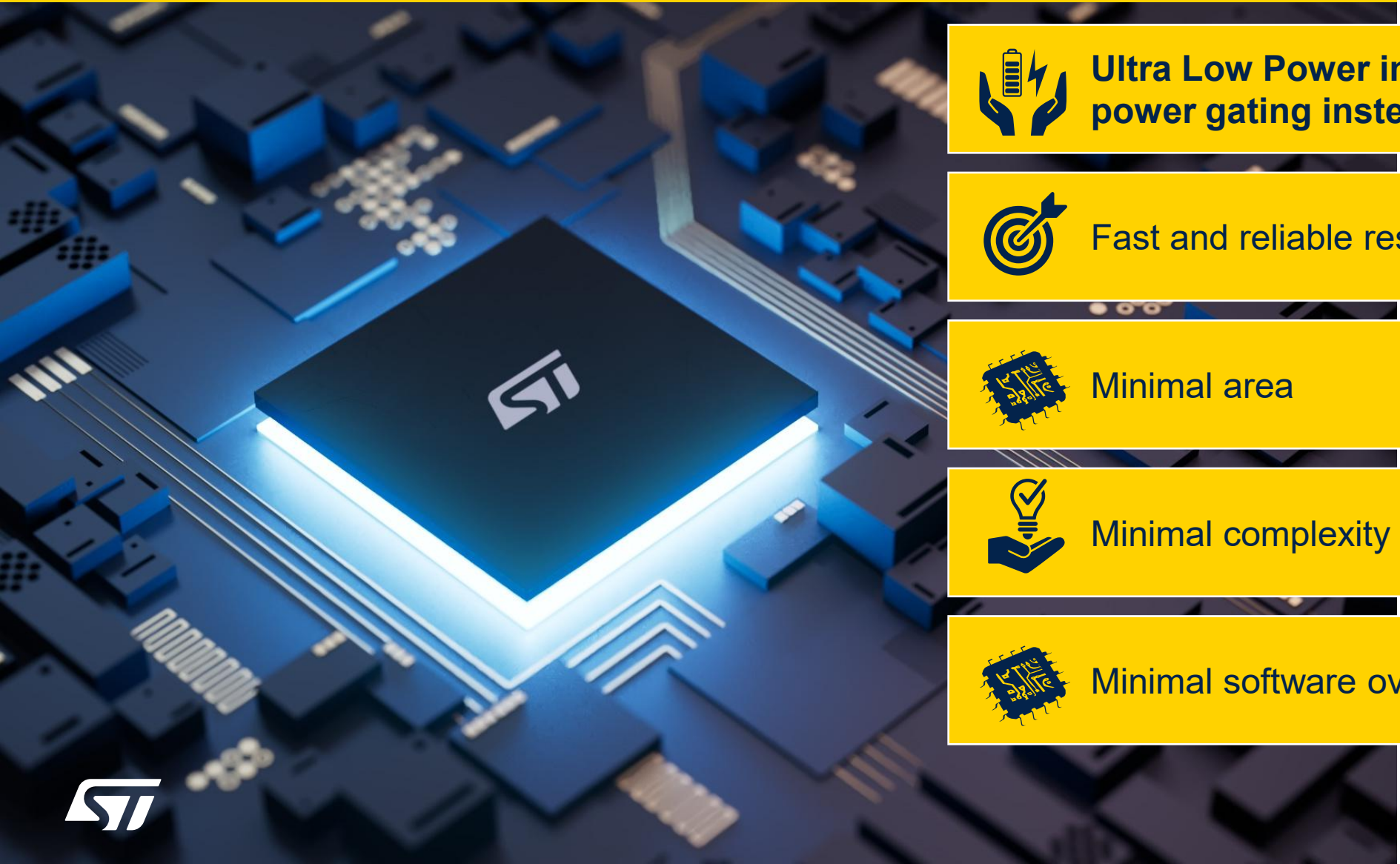
The Real Challenge

Sleeping is easy. Waking up is hard.



- **Ultra Low Power in idle: power gating instead of clock gating**
- Fast and reliable restart
- Minimal area
- Minimal complexity
- Minimal software overhead

The Common Compromise

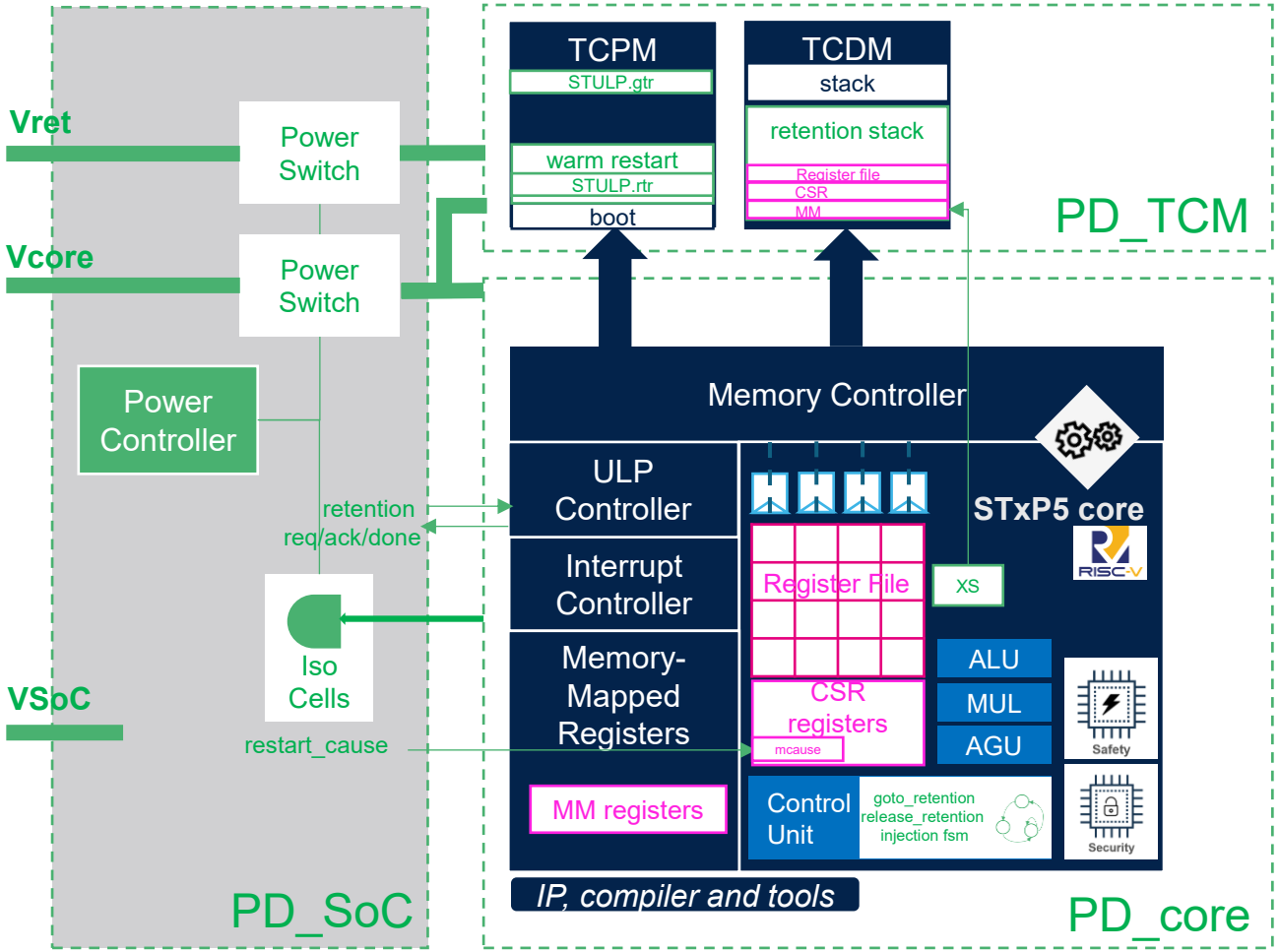
Retention flip-flops

Preserve state

Increase:

- chip area
- design complexity
- implementation effort

ST's Approach



STxP5 in-house processor family based on RISC-V ISA

Small, deeply embedded core
Highly configurable

Optimized code size, FuSa, security, and ULP

Power Modes	Power Domains	
	PD_core	PD_TCM
Execution	ON	ON
Idle	ON	ON
Retention	**OFF**	**RETENTION**
Shutdown	OFF	OFF

Few new resources to allow complete context restored at restart

What Gets Restored

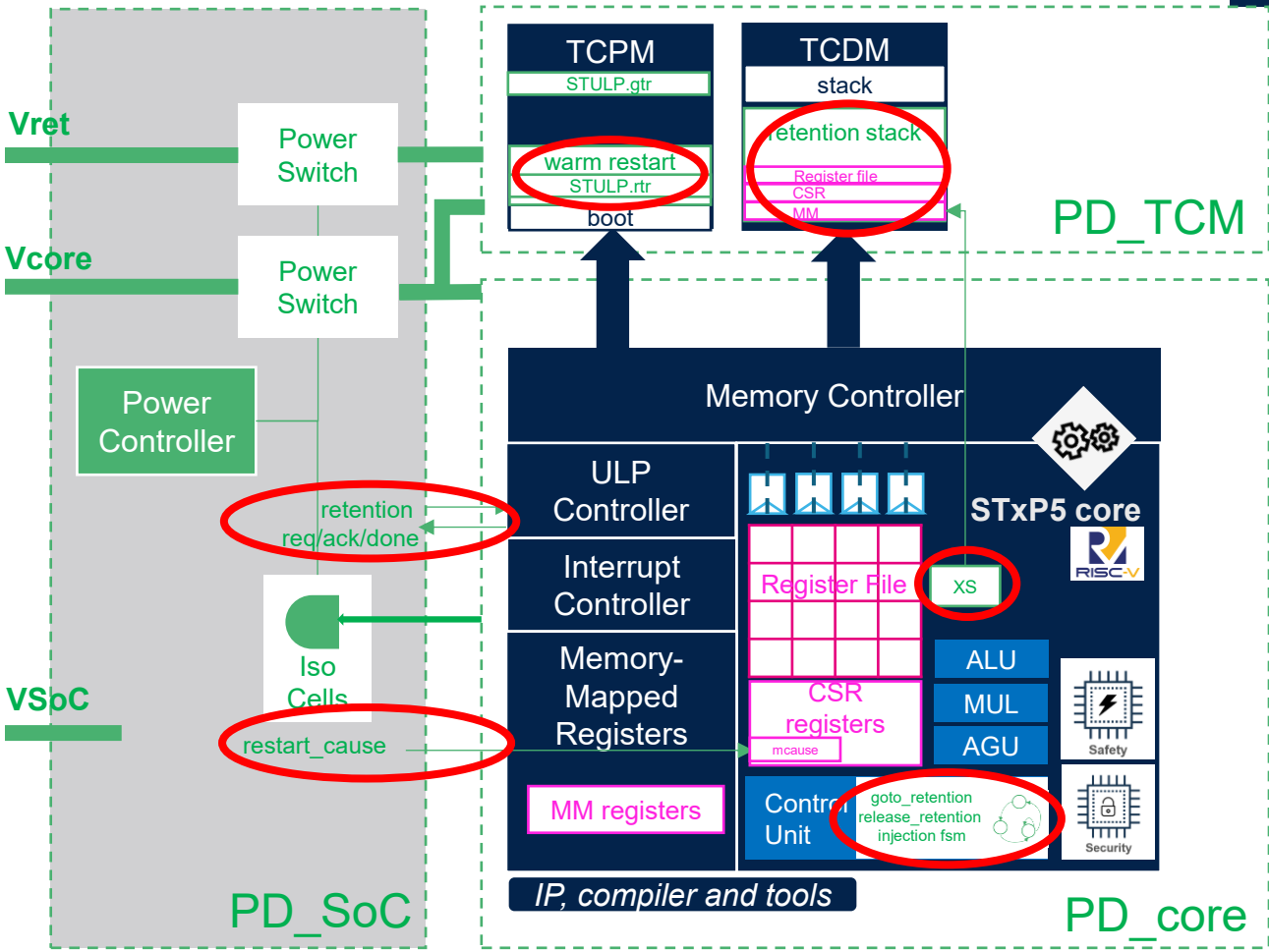
Everything the processor needs to continue

- Register file
- CSRs
- Memory-Mapped registers

Special handling for hardware-updated read-only registers like security registers

The New Resources

- a retention stack located in TCM, addressed by XS internal register
- retention request-acknowledge protocol
- restart_cause input latched at reset to indicate the restart mode
- warm restart software sequence, located in TCM
- few control logic to inject micro-instructions into the pipeline



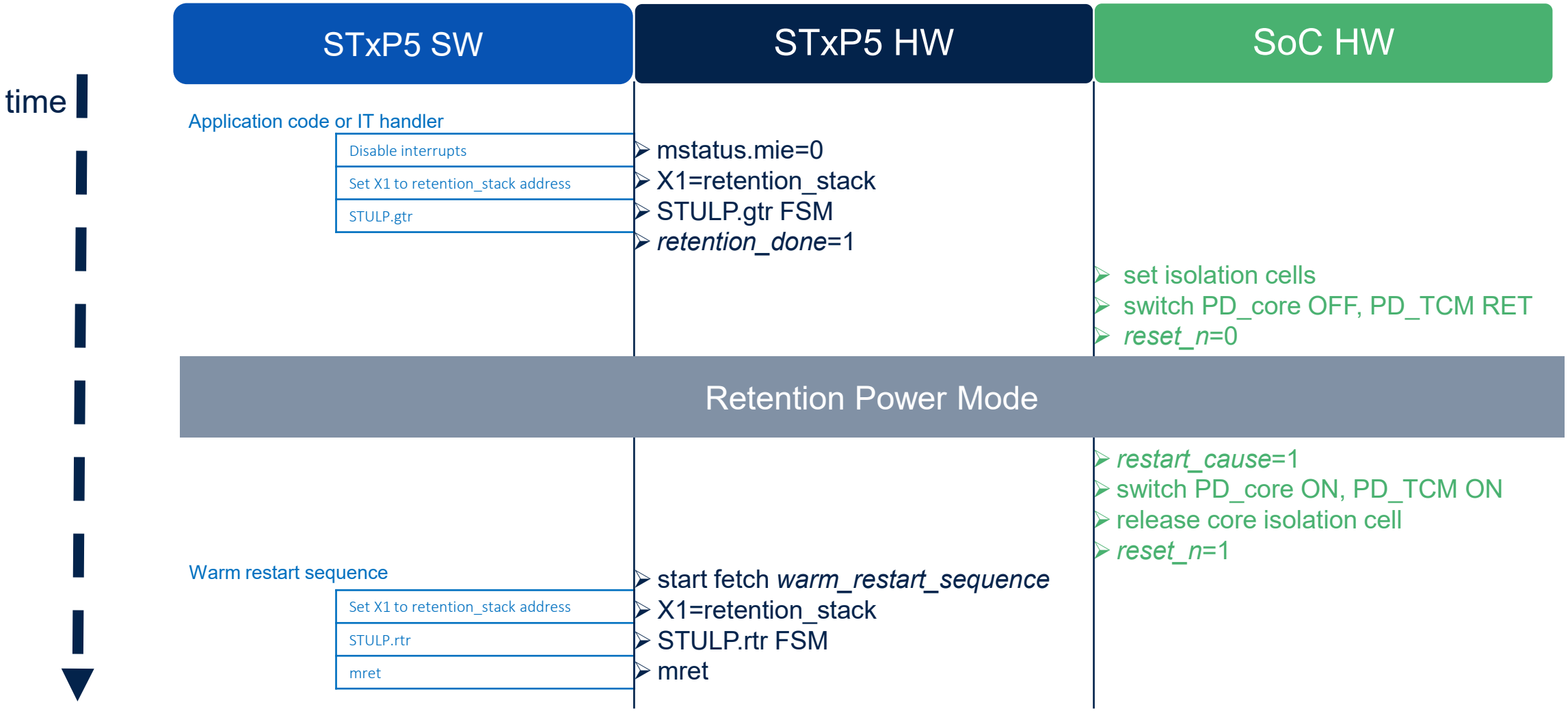
The XSTULP Extension

- 2 instructions
  - STULP.gtr — goto retention
  - STULP.rtr — restart from retention

- Triggering atomic sequences of instructions
  - Halt instruction fetch and complete any pending memory accesses
  - Save current status in CSR
  - Initialize XS
  - Save CPU context to retention stack / Restore CPU context in reverse order

  Injecting optimized, low latency micro-instructions to handle register access and updates, load/store operations, and XS pre-decrement/post-increment

How it Works


time
STxP5 SW
STxP5 HW
SoC HW
Application code or IT handler
Disable interrupts
Set X1 to retention_stack address
STULP.gtr
mstatus.mie=0
X1=retention_stack
STULP.gtr FSM
retention_done=1
set isolation cells
switch PD_core OFF, PD_TCM RET
reset_n=0
Retention Power Mode
restart_cause=1
switch PD_core ON, PD_TCM ON
release core isolation cell
reset_n=1
Warm restart sequence
Set X1 to retention_stack address
STULP.rtr
mret
start fetch warm_restart_sequence
X1=retention_stack
STULP.rtr FSM
mret

The Results

Full

context recovery

Ultra-low power with practical benefits

Power limited to TCM leakage
~40× lower total power than idle mode

Resume time about **2× faster** than cold restart partial recovery

Software cost: **< 10 instructions**
STxP5 toolset provides HAL functions

Hardware cost: **< 3 kEqG + retention stack**

Verification and Robustness

Dynamic verification

UPF aware dynamic verification

- Full verification test suite - architecture tests, self-check random tests, benchmarks, application
- Execution trace comparison versus RISC-V Golden Reference Model
- 100% RTL code and functional coverage

Formal verification

UPF aware formal verification

- Micro-architecture properties verification through structural analysis
- Coverage unreachability verification

Designed to be trusted

Conclusion

Ultra-low power “power OFF” as **simple** as “clock OFF”

Automatic full and **fast** resume at a modest hardware and software cost

Custom **RISC-V extension**

For a **smart** and **warm restart**

Our technology starts with You

Find out more at www.st.com