RISC-V Custom Instructions for Automotive Control and DSP Algorithms Compliant with ISO 26262

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Chapter 1
Introduction

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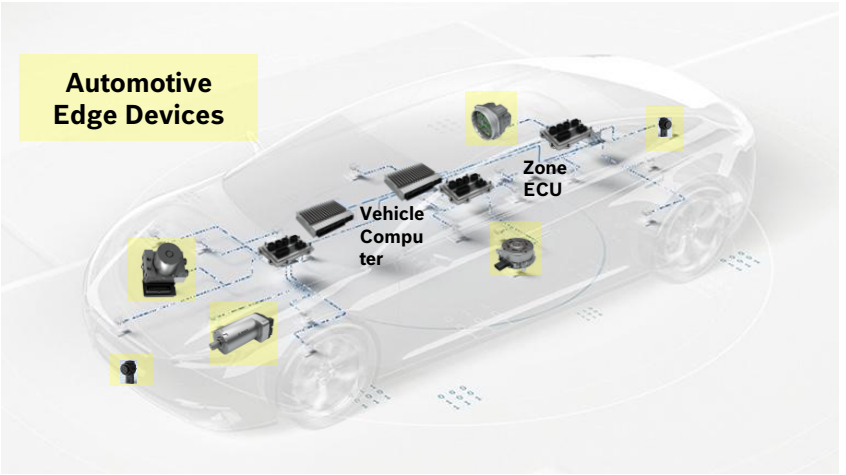
Introduction

- Specific requirements for processors in **automotive edge devices**
  - **Examples:** Sensors (inertial, ultrasonic, radar), actuators (steering, wiper, thermomanagement)
  - **Cost / area:** Processor silicon area must be tightly controlled to meet cost targets
  - **Efficiency (PPA):** Strong performance with low power and minimal area
  - **Functional safety:** Designs must support ISO 26262 and address both systematic faults and random hardware faults



- **Challenge:** Fullfilling efficiency requirements while keeping functional safety
  - **RISC-V custom instructions:** Optimizing the processor for targeted workloads
  - Safety compliance of processors typically performed for **limited amount of configurations**

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Custom Instructions and Their Impact on Certification

- **Certification must be re-evaluated**
  - Custom instructions can introduce new failure modes
  - Changes of safety-critical functions require new certification process

- **What does that mean?**
  - Custom instructions can introduce systematic faults as well as new random faults
  - Requires new assessment of random fault detection
  - Requires re-verification of the design

- **ISO 26262-5:2018:** Road vehicles - Functional safety - Part 5: Product development at Hardware Level
  - Clause 4 + 7: RTL changes must be re-evaluated and re-certified under the compliance framework with the highest ASIL
  - Clause 9: Evaluation of Each Cause (EEC) and its impact on safety goals has to be conducted

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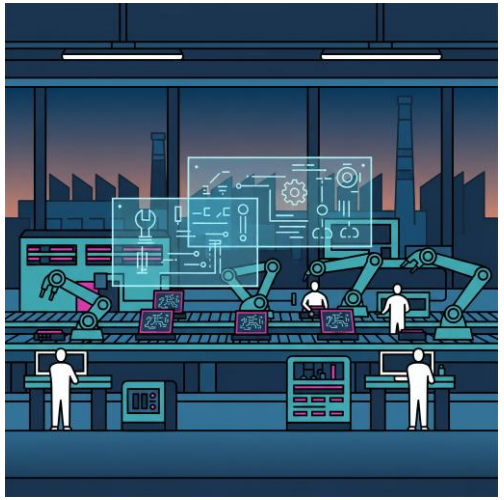
State of the Art: Extendable Processor Solutions



- Classic processor generation toolchains
  - Automated processor and toolchain generation based on DSL
  - Allows optimization of processors to specific applications
  - Complete certification of the generated solutions have to be done by user

- Certified RISC-V Processors with Custom Extension Interface
  - Fixed and certified processor IP
  - Custom instruction interfaces are complex, custom instructions share resources, failure modes can propagate into original processor IP
  - Processors have to be recertified as custom instructions are added

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Chapter 2

Codasip Bounded Customization

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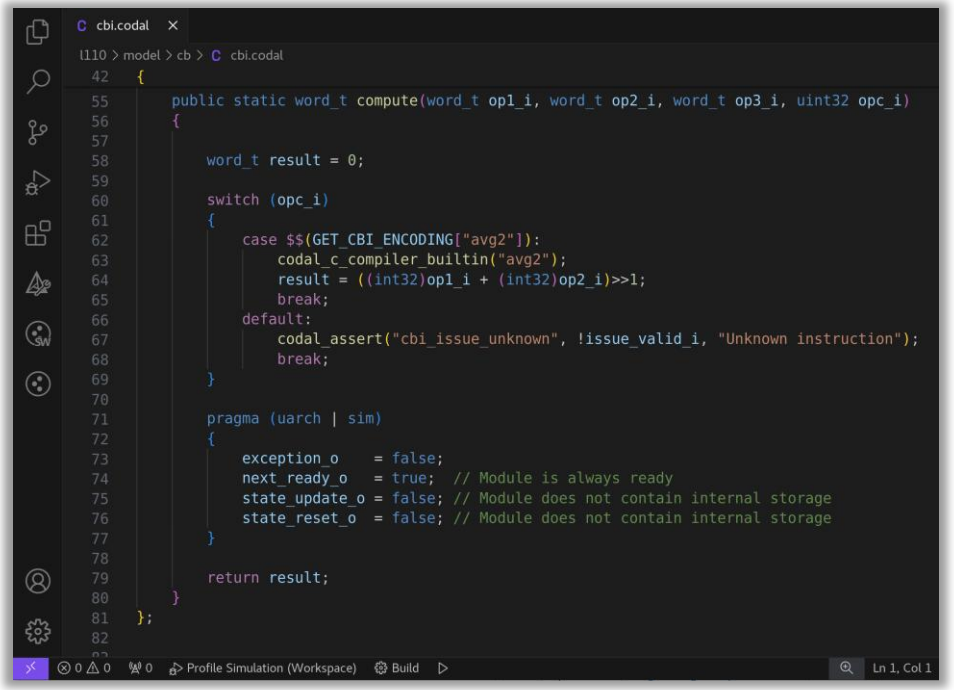
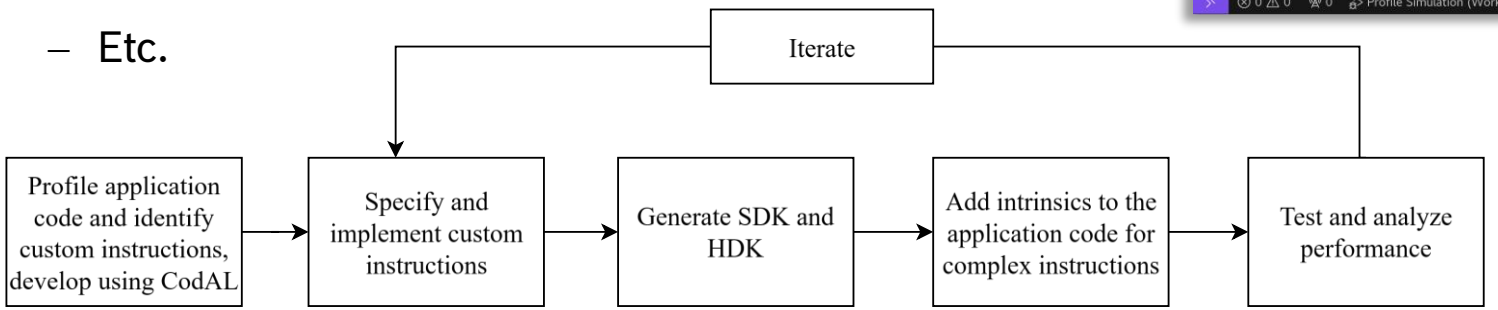
Codasip Studio: Processor Design Tool

- **Purpose**
  - Processor design and customization
- **Source**
  - Processor designed in CodAL
- **Automated generation** of custom SDK and HDK
  - LLVM based toolchain
  - Various SystemC simulators
  - RTL
  - Verification
  - Etc.



Picture: Codasip



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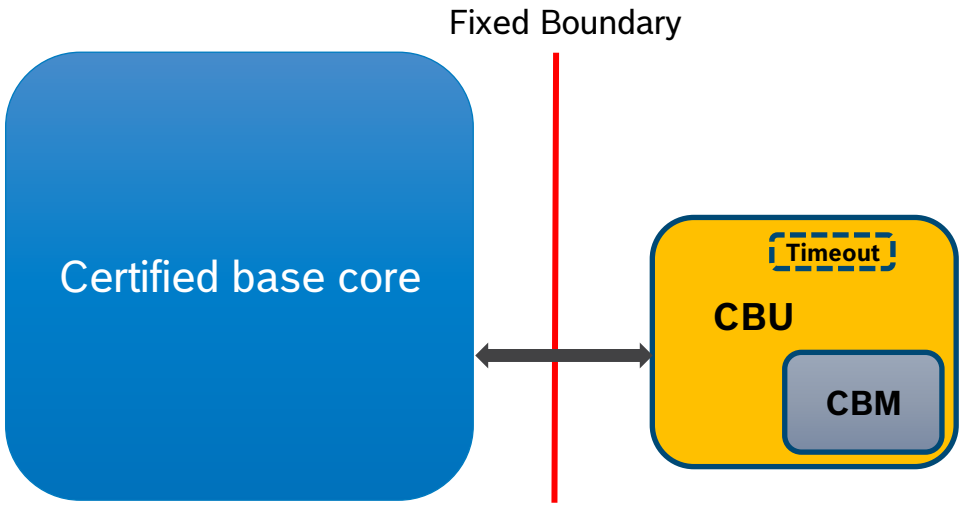
Codasip Safety Assurance Approach: Bounded Customization

- **Motivation**
  - Easier certification of the custom instructions
- **Concept**
  - Adds custom instructions to the core as a separate RTL module (Custom Bounded Module)
  - Fixed and well-defined interface between CBM (Custom Bounded Module) and the processor
  - Studio checks the new instructions and makes sure that they are compliant with the pre-defined bounds
  - Bounds are formed by eight simple rules, such as that the instruction must finish in a given number of clock cycles or that the instructions must not use CSR register with a side-effect
- **Availability**
  - Pilot processor for the bounded customization concept: L110 processor



CBI – Custom Bounded Instruction
CBM – Custom Bounded Module
CBU – Custom Bounded Unit

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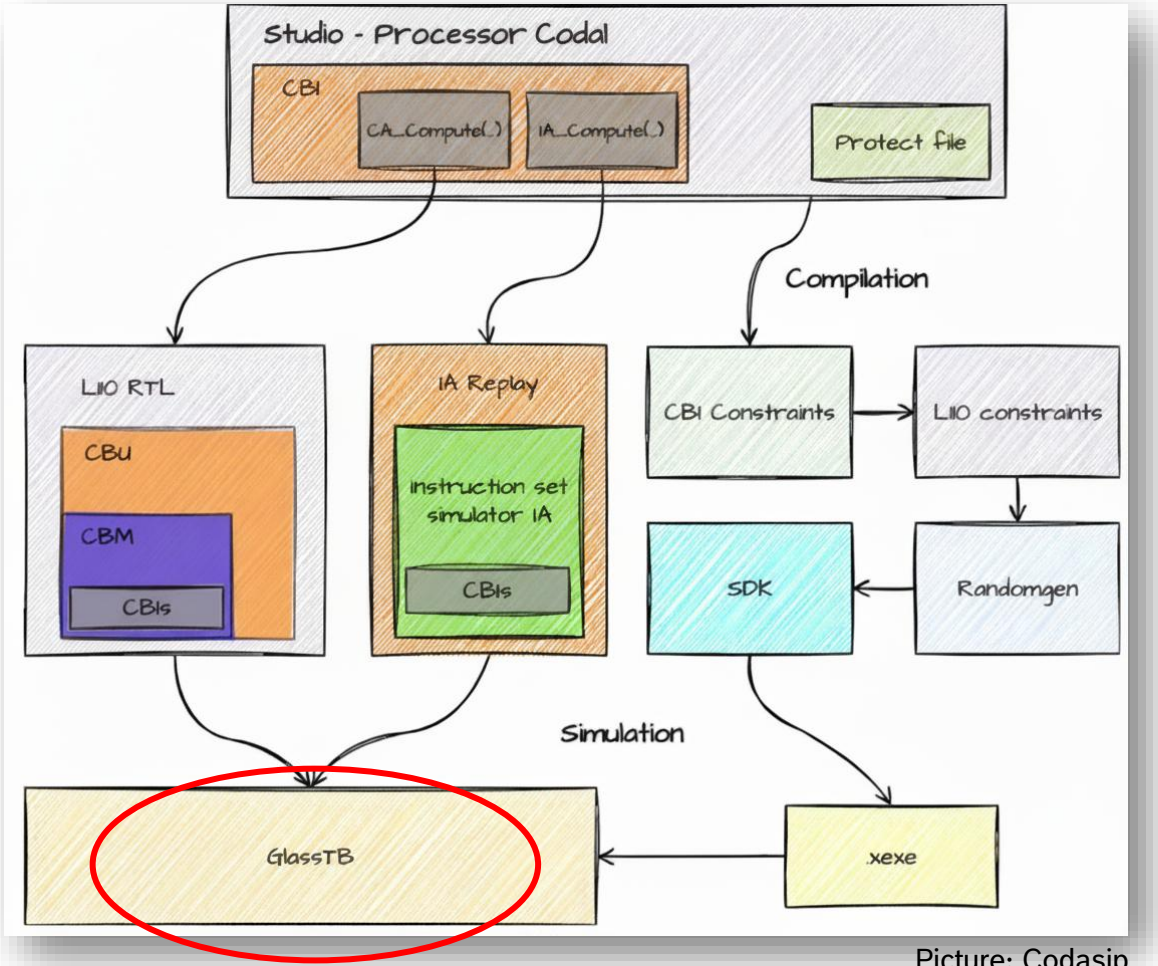
How to Design and Verify a Custom Bounded Instruction?

- **Implementation of new instructions in Studio**
  - Implemented in Codal
    - Shared or separate handling for IA and CA implementation
  - Base processor comes with a protection file that checks whether the instructions are in defined bounds

- **Codasip Studio Output**
  - RTL with custom instructions
  - Various IA/CA simulators
  - LLVM toolchain
  - Generated constraints for a random program generator to stress new instructions

- **Verification**
  - Integration of RTL and IA replay simulator (reference model)
  - Random programs generated using the generated constrains
  - Run programs and check the results on RTL and IA Replay model
  - Formal verification



Picture: Codasip

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Chapter 4
Case Study

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Case Study - Overview

Target

- Evaluation of Codasip Bounded Customization approach for automotive edge devices

Tasks

- Safety evaluation with functional safety experts
- Analysis of representative algorithms of automotive applications
- Implementation of custom instructions
- Performance / area analysis of custom instructions

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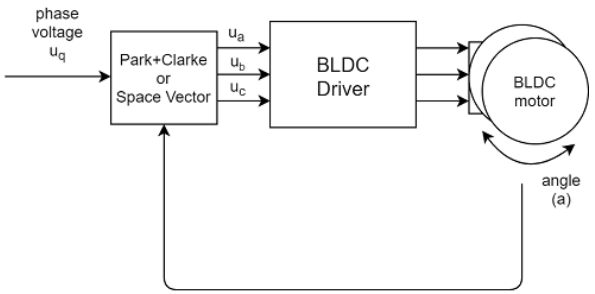
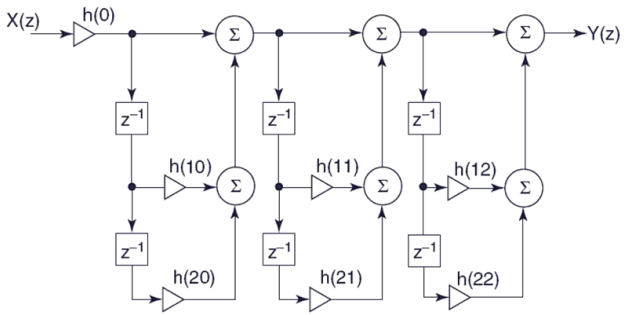
Case Study: Custom Instructions



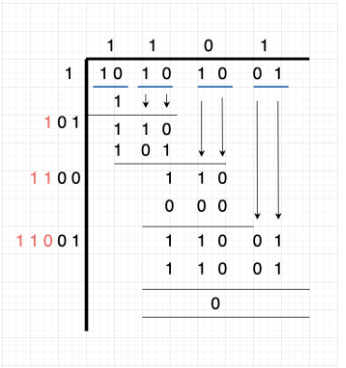
Motor Control

- Algorithm
  - Field oriented control (LUT-based)
- Custom instructions
  - Pre- and post-processing of LUT accesses



Sensor Signal Processing

- Algorithm
  - FIR filter
- Custom instructions
  - MAC with Shift



Sensor Signal Processing

- Algorithm
  - Binary square root
- Custom instructions
  - Loop structure
  - Bit level operations

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Chapter 5
Results

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Safety Evaluation of Bounded Customization

- Review with Bosch FuSa experts: Codasip presented their bounded customization concept, showing how processors can be extended with custom instructions in a controlled manner

- They explained their verification strategy for ensuring that custom instructions do not compromise the baseline RTL of the core. This includes:
  - Timeout mechanisms to detect deadlocks or hangs
  - Protocol checkers for interface compliance
  - X-propagation analysis to catch indeterminate states
  - Additional verification hooks to monitor the safety impact of customization

Outcome: The methodology appeared **consistent with functional safety principles** and provided confidence in the feasibility of bounded customization for safety-relevant designs

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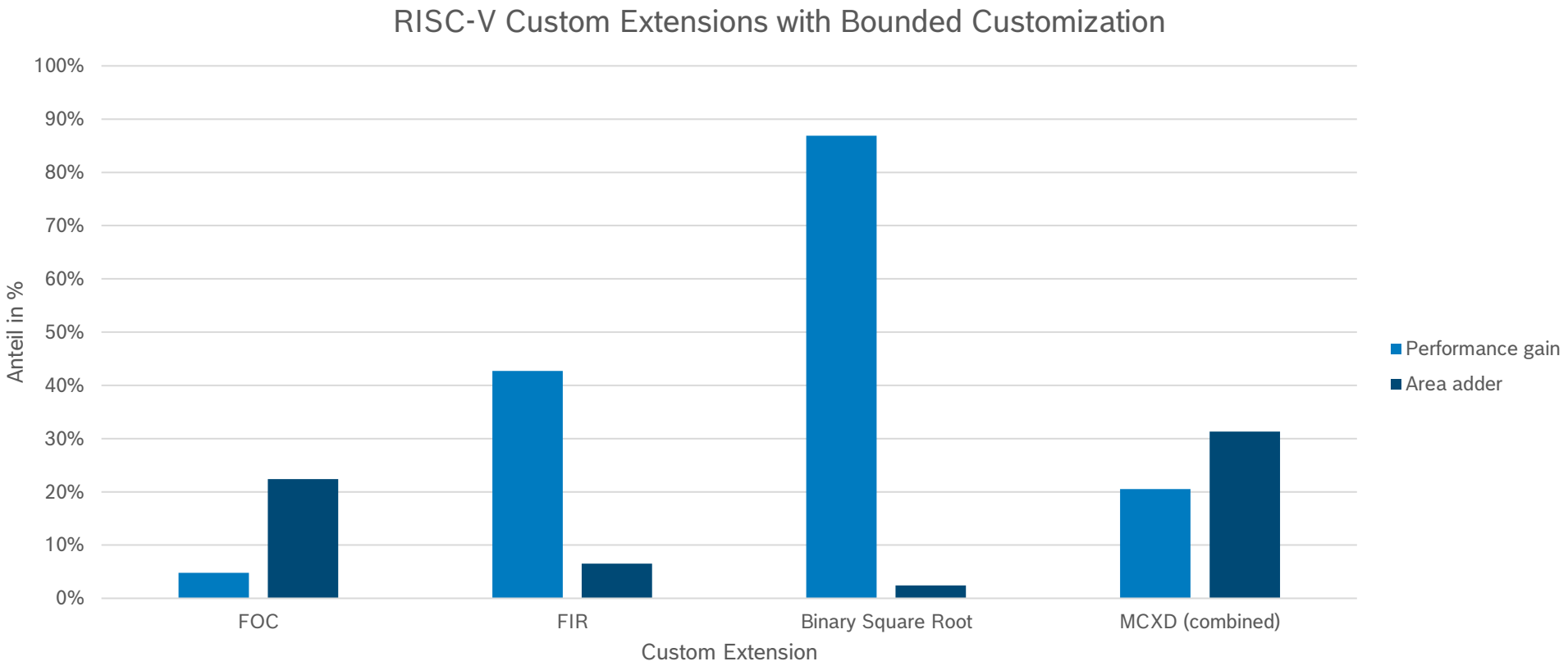
Performance and Area Results



Chapter 8
Conclusion and Outlook

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Conclusion and Outlook

- **Codasip Bounded Customization:** Fast workflow for optimized processor efficiency while keeping ISO 26262 certification

- **Bosch case study**
  - Implemented **various custom extensions** for **automotive applications** with Codasip workflow
  - Performed **performance and area analysis** as well as **functional safety review**

- **Results**
  - **Successful safety review:** Freedom of interference of custom extensions could be successfully shown
  - **Performance and area analysis:** Good performance increase with limited area adder

- **Outlook**
  - Methodology for identifying **ideal set of custom extensions** for specific applications